Ultra37000: December 13, 1996
Revision: March 15, 2001

CYPRESS

Ultra37000™ CPLD Family

5V, 3.3V, ISR™ High-Performance CPLDs

Features

- **In-System Reprogrammable™ (ISR™) CMOS CPLDs**
  - **—JTAG interface for reconfigurability**
  - **—Design changes don't cause pinout changes**
  - **—Design changes don't cause timing changes**
- **High density**
  - **—32 to 512 macrocells**
  - **—32 to 264 I/O pins**
  - **—5 dedicated inputs including 4 clock pins**
- **Simple timing model**
  - **—No fanout delays**
  - **—No expander delays**
  - **—No dedicated vs. I/O pin delays**
  - **—No additional delay through PIM**
  - **—No penalty for using full 16 product terms**
  - **—No delay for steering or sharing product terms**
- **3.3V and 5V versions**
- **PCI Compatible**[1]
- **Programmable Bus-Hold capabilities on all I/Os**
- **Intelligent product term allocator provides:**
  - **—0 to 16 product terms to any macrocell**
  - **—Product term steering on an individual basis**
  - **—Product term sharing among local macrocells**
- **Flexible clocking**
  - **—4 synchronous clocks per device**
  - **—Product Term clocking**
  - **—Clock polarity control per logic block**
- **Consistent package/pinout offering across all densities**
  - **—Simplifies design migration**
  - **—Same pinout for 3.3V and 5.0V devices**
- **Packages**
  - **—44 to 400 Leads in PLCC, CLCC, PQFP, TQFP, CQFP, BGA, and Fine-Pitch BGA packages**

General Description

The Ultra37000™ family of CMOS CPLDs provides a range of high-density programmable logic solutions with unparalleled system performance. The Ultra37000 family is designed to bring the flexibility, ease of use, and performance of the 22V10 to high-density CPLDs. The architecture is based on a number of logic blocks that are connected by a Programmable Interconnect Matrix (PIM). Each logic block features its own product term array, product term allocator, and 16 macrocells. The PIM distributes signals from the logic block outputs and all input pins to the logic block inputs.

All of the Ultra37000 devices are electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows, thereby reducing costs. The ISR feature provides the ability to reconfigure the devices without having design changes cause pinout or timing changes. The Cypress ISR function is implemented through a JTAG-compliant serial interface. Data is shifted in and out through the TDI and TDO pins, respectively. Because of the superior routability and simple timing model of the Ultra37000 devices, ISR allows users to change existing logic designs while simultaneously fixing pinout assignments and maintaining system performance.

The entire family features JTAG for ISR and boundary scan, and is compatible with the PCI Local Bus specification, meeting the electrical and timing requirements. The Ultra37000 family features user programmable bus-hold capabilities on all I/Os.

Ultra37000 5.0V Devices

The Ultra37000 devices operate with a 5V supply and can support 5V or 3.3V I/O levels. V_{CCO} connections provide the capability of interfacing to either a 5V or 3.3V bus. By connecting the V_{CCO} pins to 5V the user insures 5V TTL levels on the outputs. If V_{CCO} is connected to 3.3V the output levels meet 3.3V JEDEC standard CMOS levels and are 5V tolerant. These devices require 5V ISR programming.

Ultra37000V 3.3V Devices

Devices operating with a 3.3V supply require 3.3V on all V_{CCO} pins, reducing the device's power consumption. These devices support 3.3V JEDEC standard CMOS output levels, and are 5V tolerant. These devices allow 3.3V ISR programming.

Note:

1. Due to the 5V-tolerant nature of 3.3V device I/Os, the I/Os are not clamped to V_{CC}, PCI V_{IH}=2V.

Selection Guide

5.0V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032	32	5	32	6	200
CY37064	64	5	32/64	6	200
CY37128	128	5	64/128	6.5	167
CY37192	192	5	120	7.5	154
CY37256	256	5	128/160/192	7.5	154
CY37384	384	5	160/192	10	118
CY37512	512	5	160/192/264	10	118

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032	X		X		X			
CY37064	X		X		X			
CY37128		X			X	X		
CY37192			X		X		X	
CY37256			X		X		X	
CY37384					X		X	
CY37512					X	X	X	

Device-Package Offering & I/O Count

Device	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	256-Lead BGA	352-Lead BGA
CY37032	37	37										
CY37064	37	37	37	69		69						
CY37128				69	69	69	133					
CY37192							125					
CY37256							133	133	165		197	
CY37384									165		197	
CY37512									165	165	197	269

3.3V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032V	32	5	32	8.5	143
CY37064V	64	5	32/64	8.5	143
CY37128V	128	5	64/80/128	10	125
CY37192V	192	5	120	12	100
CY37256V	256	5	128/160/192	12	100
CY37384V	384	5	160/192	15	83
CY37512V	512	5	160/192/264	15	83

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032V				X		X		
CY37064V				X		X		
CY37128V				X	X		X	
CY37192V						X		X
CY37256V				X		X		X
CY37384V							X	X
CY37512V					X		X	X

Shaded areas indicate preliminary speed bins.

Device-Package Offering & I/O Count

Device	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	48-Lead FBGA	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	100-Lead FBGA	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	256-Lead BGA	256-Lead FBGA	352-Lead BGA	400-Lead FBGA
CY37032V	37	37		37												
CY37064V	37	37	37	37	69		69	69								
CY37128V					69	69	69	85	133							
CY37192V									125							
CY37256V									133	133	165		197	197		
CY37384V											165		197			
CY37512V											165	165	197		269	269

Architecture Overview of Ultra37000 Family

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) consists of a completely global routing matrix for signals from I/O pins and feedbacks from the logic blocks. The PIM provides extremely robust interconnection to avoid fitting and density limitations.

The inputs to the PIM consist of all I/O and dedicated input pins and all macrocell feedbacks from within the logic blocks. The number of PIM inputs increases with pin count and the number of logic blocks. The outputs from the PIM are signals routed to the appropriate logic blocks. Each logic block receives 36 inputs from the PIM and their complements, allowing for 32-bit operations to be implemented in a single pass through the device. The wide number of inputs to the logic block also improves the routing capacity of the Ultra37000 family.

An important feature of the PIM is its simple timing. The propagation delay through the PIM is accounted for in the timing specifications for each device. There is no additional delay for traveling through the PIM. In fact, all inputs travel through the PIM. As a result, there are no route-dependent timing parameters on the Ultra37000 devices. The worst-case PIM delays are incorporated in all appropriate Ultra37000 specifications.

Routing signals through the PIM is completely invisible to the user. All routing is accomplished by software—no hand routing is necessary. *Warp*™ and third-party development packages automatically route designs for the Ultra37000 family in a matter of minutes. Finally, the rich routing resources of the Ultra37000 family accommodate last minute logic changes while maintaining fixed pin assignments.

Logic Block

The logic block is the basic building block of the Ultra37000 architecture. It consists of a product term array, an intelligent product-term allocator, 16 macrocells, and a number of I/O cells. The number of I/O cells varies depending on the device used. Refer to *Figure 1* for the block diagram.

Product Term Array

Each logic block features a 72 x 87 programmable product term array. This array accepts 36 inputs from the PIM, which originate from macrocell feedbacks and device pins. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 87 product terms in the array can be created from any of the 72 inputs.

Of the 87 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Four of the remaining seven product terms in the logic block are output enable (OE) product terms. Each of the OE product terms controls up to eight of the 16 macrocells and is selectable on an individual macrocell basis. In other words, each I/O cell can select between one of two OE product terms to control the output buffer. The first two of these four OE product terms are available to the upper half of the I/O macrocells in a logic block. The other two OE product terms are available to the lower half of the I/O macrocells in a logic block.

The next two product terms in each logic block are dedicated asynchronous set and asynchronous reset product terms. The final product term is the product term clock. The set, reset, OE and product term clock have polarity control to realize OR functions in a single pass through the array.

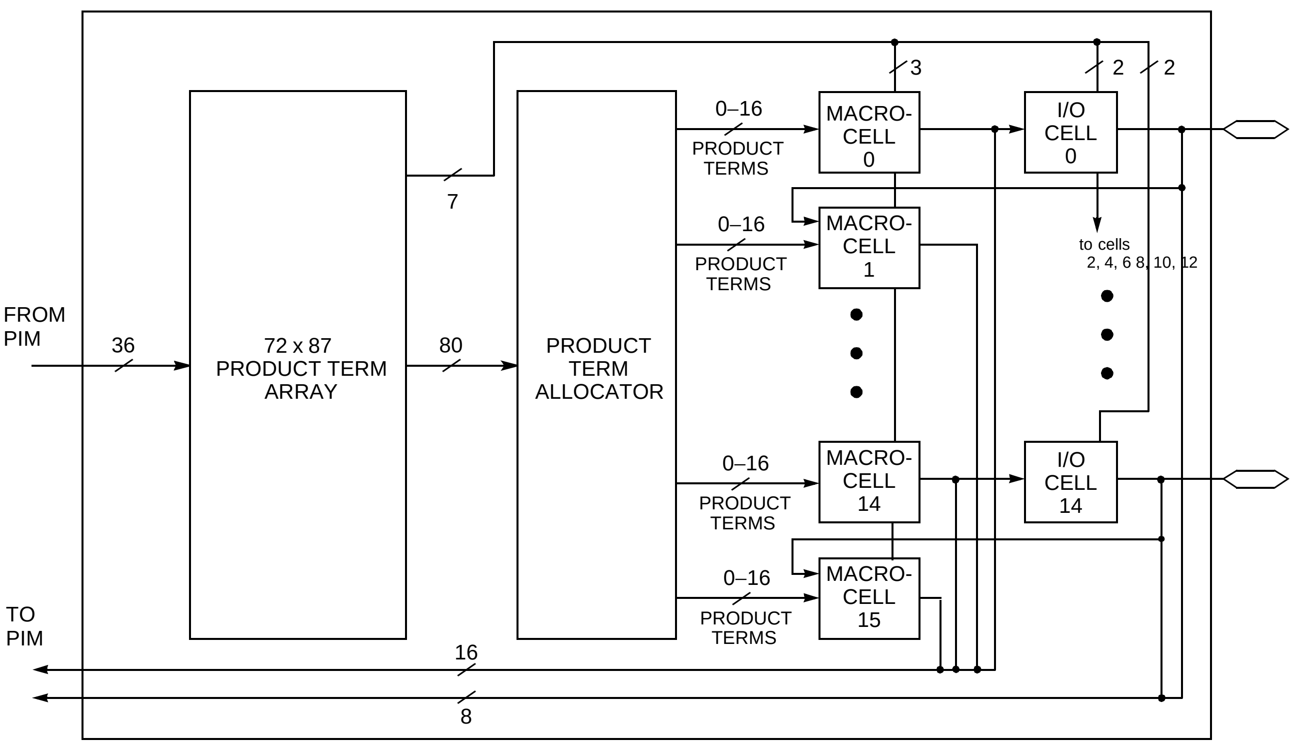


Figure 1. Logic Block with 50% Buried Macrocells

Low-Power Option

Each logic block can operate in high-speed mode for critical path performance, or in low-power mode for power conservation. The logic block mode is set by the user on a logic block by logic block basis.

Product Term Allocator

Through the product term allocator, software automatically distributes product terms among the 16 macrocells in the logic block as needed. A total of 80 product terms are available from the local product term array. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will “steer” ten product terms to one macrocell and three to the other. On Ultra37000 devices, product terms are steered on an individual basis. Any number between 0 and 16 product terms can be steered to any macrocell. Note that 0 product terms is useful in cases where a particular macrocell is unused or used as an input register.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one output has one or more product terms in its equation that are common to other outputs, those product terms are only programmed once. The Ultra37000 product term allocator allows sharing across groups of four output macrocells in a variable fashion. The software automatically takes advantage of this capability—the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All worst-case steering and sharing configurations have been incorporated in the timing specifications for the Ultra37000 devices.

Ultra37000 Macrocell

Within each logic block there are 16 macrocells. Macrocells can either be I/O Macrocells, which include an I/O Cell which is associated with an I/O pin, or buried Macrocells, which do not connect to an I/O. The combination of I/O Macrocells and buried Macrocells varies from device to device.

Buried Macrocell

Figure 2 displays the architecture of buried macrocells. The buried macrocell features a register that can be configured as combinatorial, a D flip-flop, a T flip-flop, or a level-triggered latch.

The register can be asynchronously set or asynchronously reset at the logic block level with the separate set and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be set or reset based on an AND expression or an OR expression.

Clocking of the register is very flexible. Four global synchronous clocks and a product term clock are available to clock the register. Furthermore, each clock features programmable polarity so that registers can be triggered on falling as well as rising edges (see the Clocking section). Clock polarity is chosen at the logic block level.

The buried macrocell also supports input register capability. The buried macrocell can be configured to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

I/O Macrocell

Figure 2 illustrates the architecture of the I/O macrocell. The I/O macrocell supports the same functions as the buried macrocell with the addition of I/O capability. At the output of the macrocell, a polarity control mux is available to select active LOW or active HIGH signals. This has the added advantage of allowing significant logic reduction to occur in many applications.

The Ultra37000 macrocell features a feedback path to the PIM separate from the I/O pin input path. This means that if the macrocell is buried (fed back internally only), the associated I/O pin can still be used as an input.

Bus Hold Capabilities on all I/Os

Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device’s performance. As a latch, bus-hold maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND. For more information, see the application note “Understanding Bus-Hold – A Feature of Cypress CPLDs.”

Programmable Slew Rate Control

Each output has a programmable configuration bit, which sets the output slew rate to fast or slow. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.

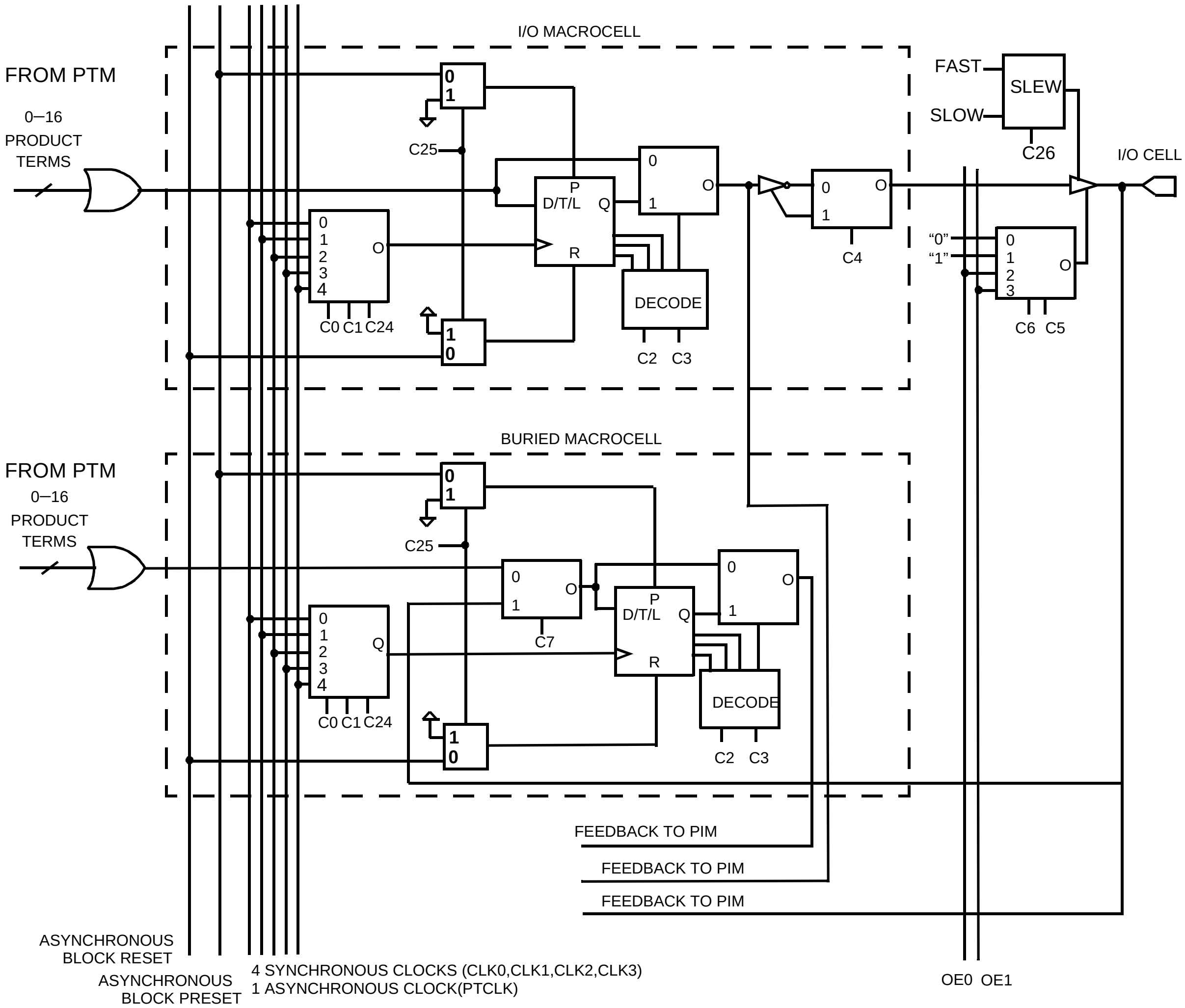


Figure 2. I/O and Buried Macrocells

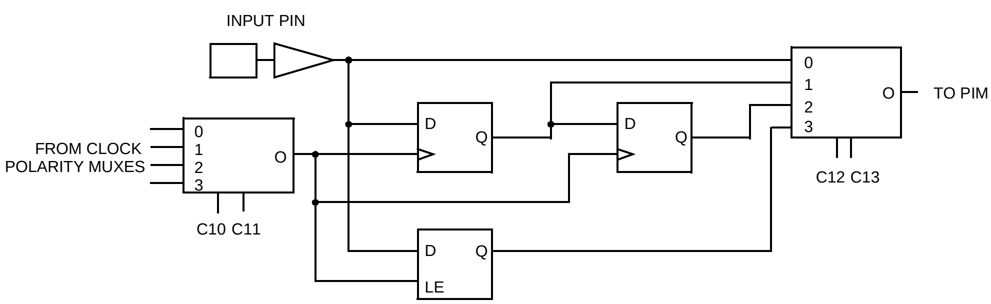


Figure 3. Input Macrocell

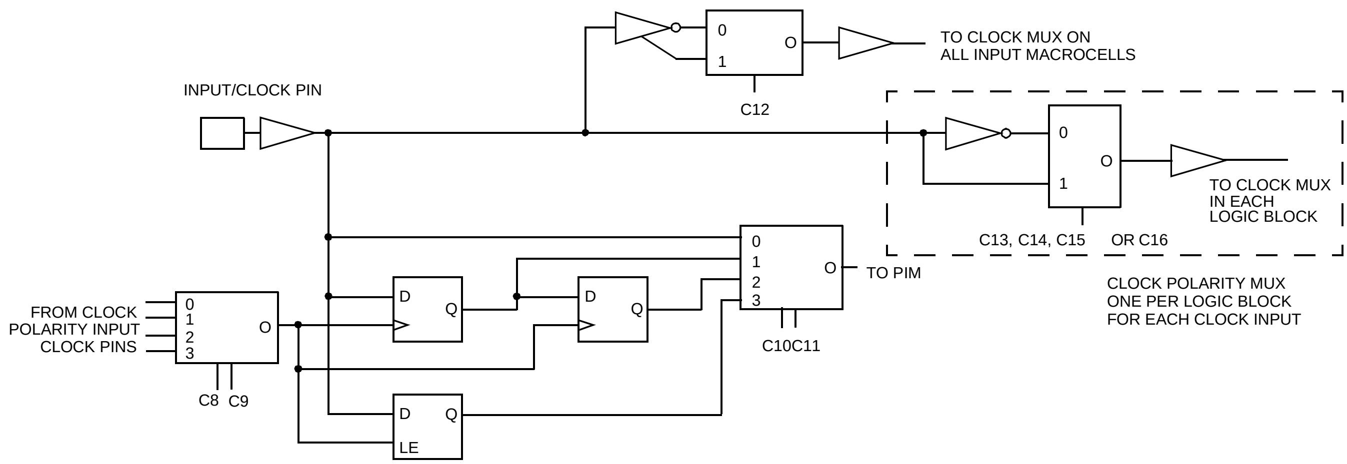


Figure 4. Input/Clock Macrocell

Clocking

Each I/O and buried macrocell has access to four synchronous clocks (CLK0, CLK1, CLK2 and CLK3) as well as an asynchronous product term clock PTCLK. Each input macrocell has access to all four synchronous clocks.

Dedicated Inputs/Clocks

Five pins on each member of the Ultra37000 family are designated as input-only. There are two types of dedicated inputs on Ultra37000 devices: input pins and input/clock pins. *Figure 3* illustrates the architecture for input pins. Four input options are available for the user: combinatorial, registered, double-registered, or latched. If a registered or latched option is selected, any one of the input clocks can be selected for control.

Figure 4 illustrates the architecture for the input/clock pins. Like the input pins, input/clock pins can be combinatorial, registered, double-registered, or latched. In addition, these pins feed the clocking structures throughout the device. The clock path at the input has user-configurable polarity.

Product Term Clocking

In addition to the four synchronous clocks, the Ultra37000 family also has a product term clock for asynchronous clocking. Each logic block has an independent product term clock which is available to all 16 macrocells. Each product term clock also supports user configurable polarity selection.

Timing Model

One of the most important features of the Ultra37000 family is the simplicity of its timing. All delays are worst case and system performance is unaffected by the features used. *Figure 5* illustrates the true timing model for the 167-MHz devices in high speed mode. For combinatorial paths, any input to any output incurs a 6.5-ns worst-case delay regardless of the amount of logic used. For synchronous systems, the input setup time to the output macrocells for any input is 3.5 ns and the clock to output time is also 4.0 ns. These measurements are for any output and synchronous clock, regardless of the logic used.

The Ultra37000 features:

- No fanout delays
- No expander delays
- No dedicated vs. I/O pin delays
- No additional delay through PIM
- No penalty for using 0–16 product terms
- No added delay for steering product terms
- No added delay for sharing product terms
- No routing delays
- No output bypass delays

The simple timing model of the Ultra37000 family eliminates unexpected performance penalties.

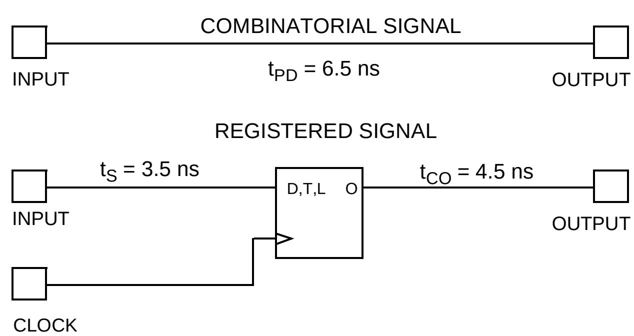


Figure 5. Timing Model for CY37128

JTAG and PCI Standards

PCI Compliance

5V operation of the Ultra37000 is fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The 3.3V products meet all PCI requirements except for the output 3.3V clamp, which is in direct conflict with 5V tolerance. The Ultra37000 family's simple and predictable timing model ensures compliance with the PCI AC specifications independent of the design.

IEEE 1149.1 Compliant JTAG

The Ultra37000 family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR.

Boundary Scan

The Ultra37000 family supports Bypass, Sample/Preload, Extest, Idcode, and Usercode boundary scan instructions. The JTAG interface is shown in *Figure 6*.

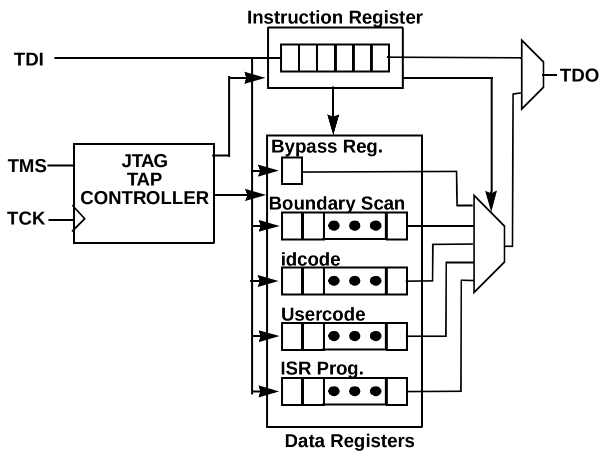


Figure 6. JTAG Interface

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Ultra37000 family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing resources for pinout flexibility, and a simple timing model for consistent system performance.

Development Software Support

Warp™

Warp is a state-of-the-art compiler and complete CPLD design tool. For design entry, *Warp* provides an IEEE-STD-1076/1164 VHDL text editor, an IEEE-STD-1364 Verilog text editor, and a graphical finite state machine editor. It provides optimized synthesis and fitting by replacing basic circuits with ones pre-optimized for the target device, by implementing logic in unused memory and by perfect communication between fitting and synthesis. To facilitate design and debugging, *Warp* provides graphical timing simulation and analysis.

Warp Professional™

Warp Professional contains several additional features. It provides an extra method of design entry with its graphical block diagram editor. It allows up to 5 ms timing simulation instead of only 2 ms. It allows comparison of waveforms before and after design changes.

Warp Enterprise™

Warp Enterprise provides even more features. It provides unlimited timing simulation and source-level behavioral simulation as well as a debugger. It has the ability to generate graphical HDL blocks from HDL text. It can even generate testbenches.

Warp is available for PC and UNIX platforms. Some features are not available in the UNIX version. For further information see the *Warp* for PC, *Warp* for UNIX, *Warp* Professional and *Warp* Enterprise data sheets on Cypress's web site (www.cypress.com).

Third-Party Software

Although *Warp* is a complete CPLD development tool on its own, it interfaces with nearly every third party EDA tool. All major third-party software vendors provide support for the Ultra37000 family of devices. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third-party vendors.

Programming

There are four programming options available for Ultra37000 devices. The first method is to use a PC with the 37000 UltraISR programming cable and software. With this method, the ISR pins of the Ultra37000 devices are routed to a connector at the edge of the printed circuit board. The 37000 UltraISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the Ultra37000 devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions. For more information on the Cypress ISR Interface, see the ISR Programming Kit data sheet (CY3700i).

The second method for programming Ultra37000 devices is on automatic test equipment (ATE). This is accomplished through a file created by the ISR software. Check the Cypress website for the latest ISR software download information.

The third programming option for Ultra37000 devices is to utilize the embedded controller or processor that already exists in the system. The Ultra37000 ISR software assists in this method by converting the device JEDEC maps into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be programmed. The embedded controller then simply directs this ISR stream to the chain of Ultra37000 devices to complete the desired reconfiguring or diagnostic operations. Contact your local sales office for information on availability of this option.

The fourth method for programming Ultra37000 devices is to use the same programmer that is currently being used to program FLASH370i devices.

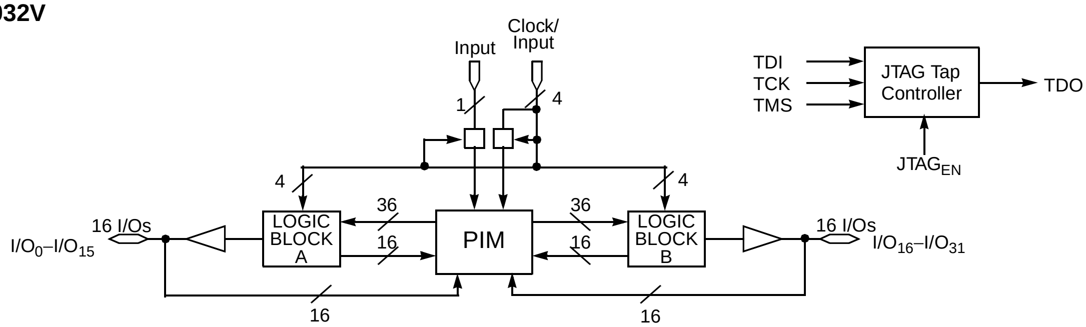
For all pinout, electrical, and timing requirements, refer to device data sheets. For ISR cable and software specifications, refer to the UltraISR kit data sheet (CY3700i).

Third-Party Programmers

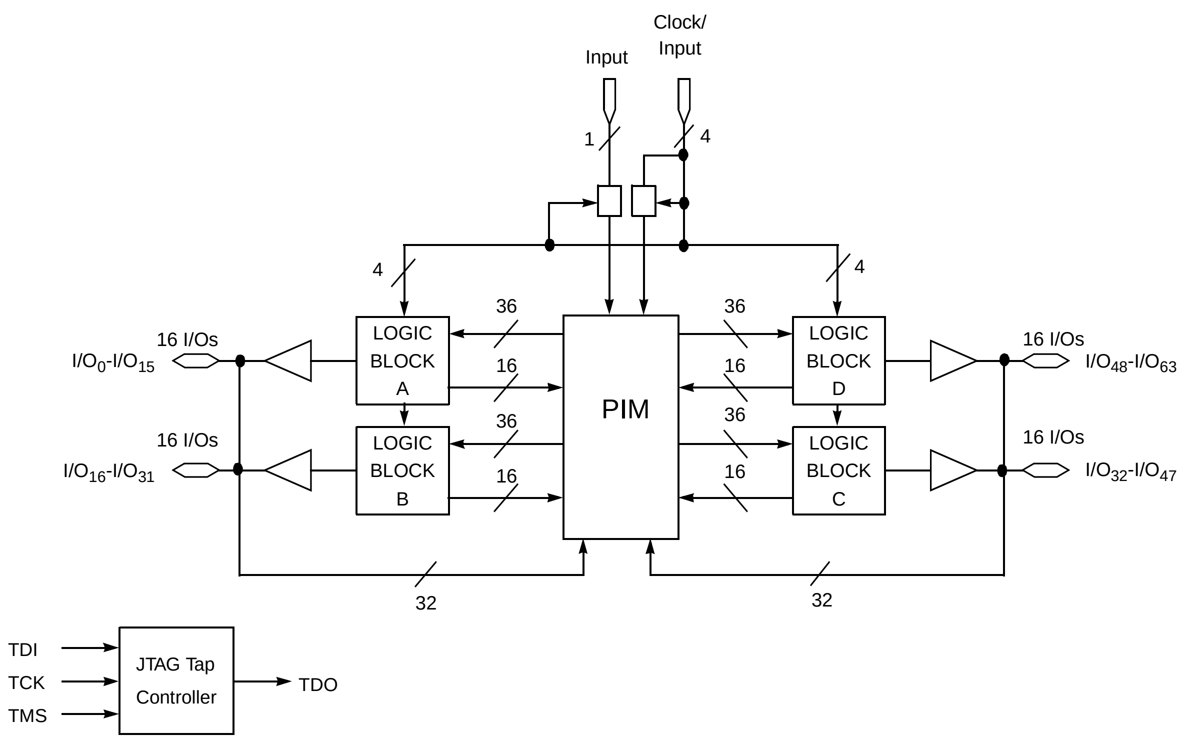
As with development software, Cypress support is available on a wide variety of third-party programmers. All major third-party programmers (including BP Micro, Data I/O, and SMS) support the Ultra37000 family.

Logic Block Diagrams

CY37032 / CY37032V

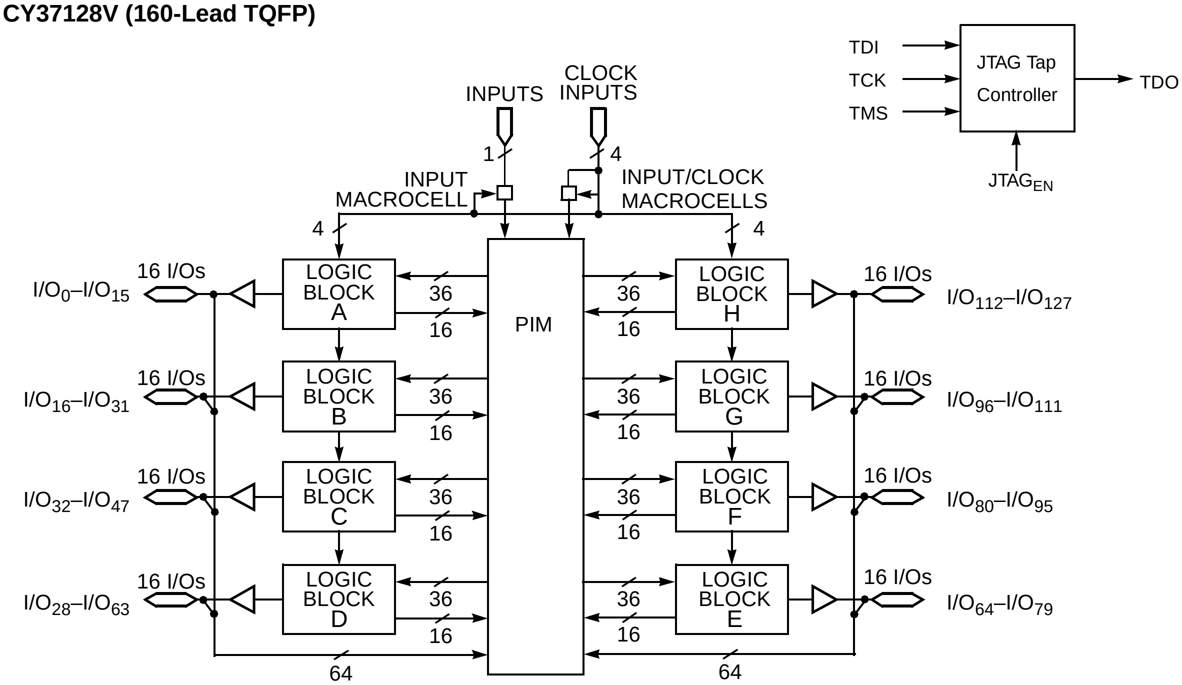


CY37064 / CY37064V (100-Lead TQFP)

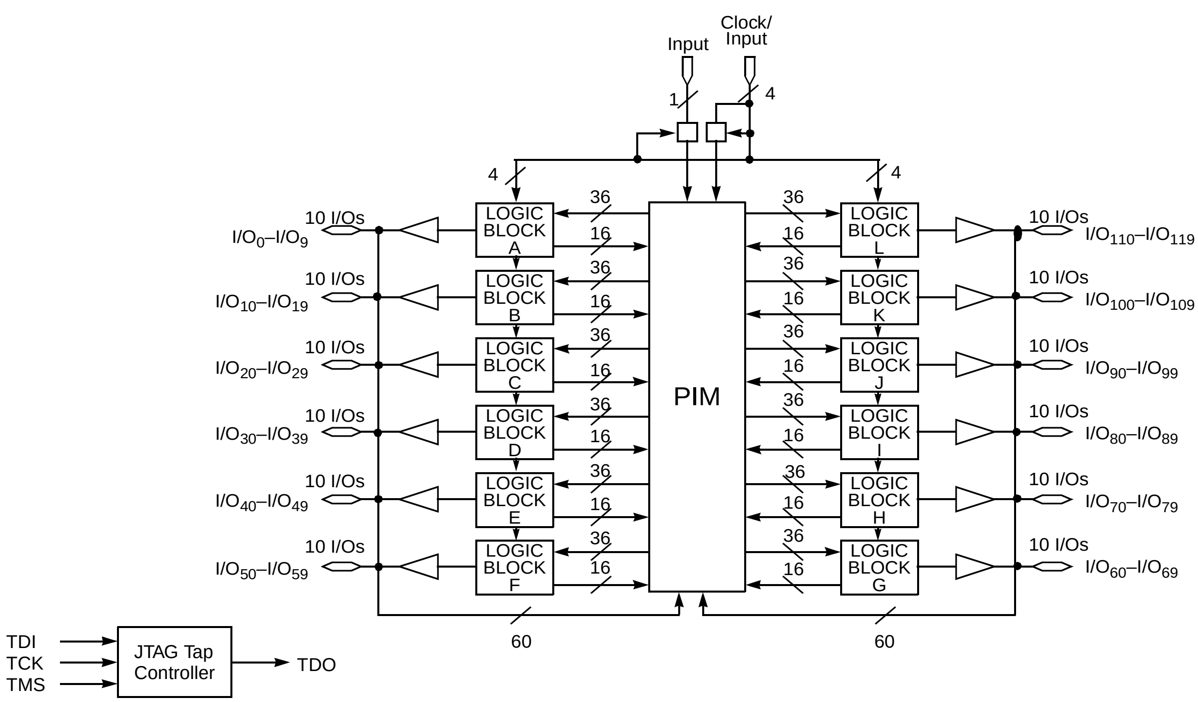


Logic Block Diagrams (continued)

CY37128 / CY37128V (160-Lead TQFP)

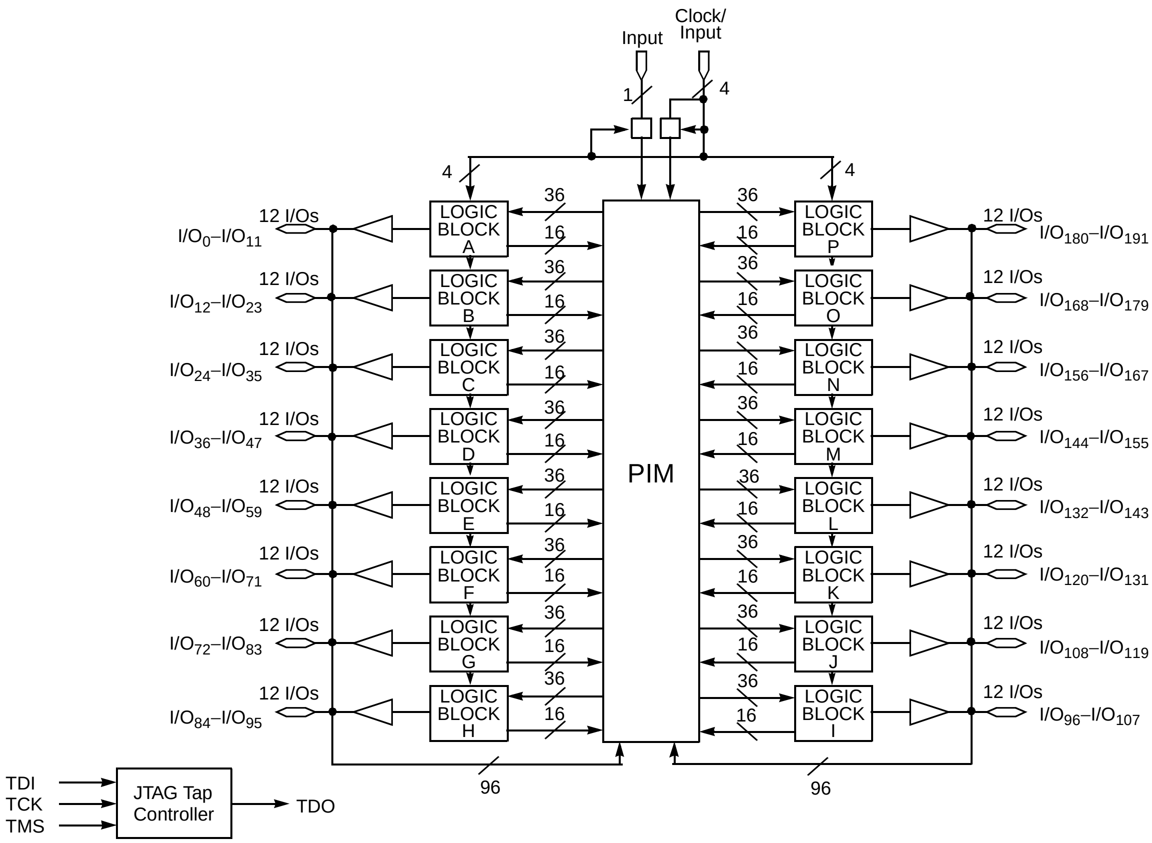


CY37192 / CY37192V (160-Lead TQFP)



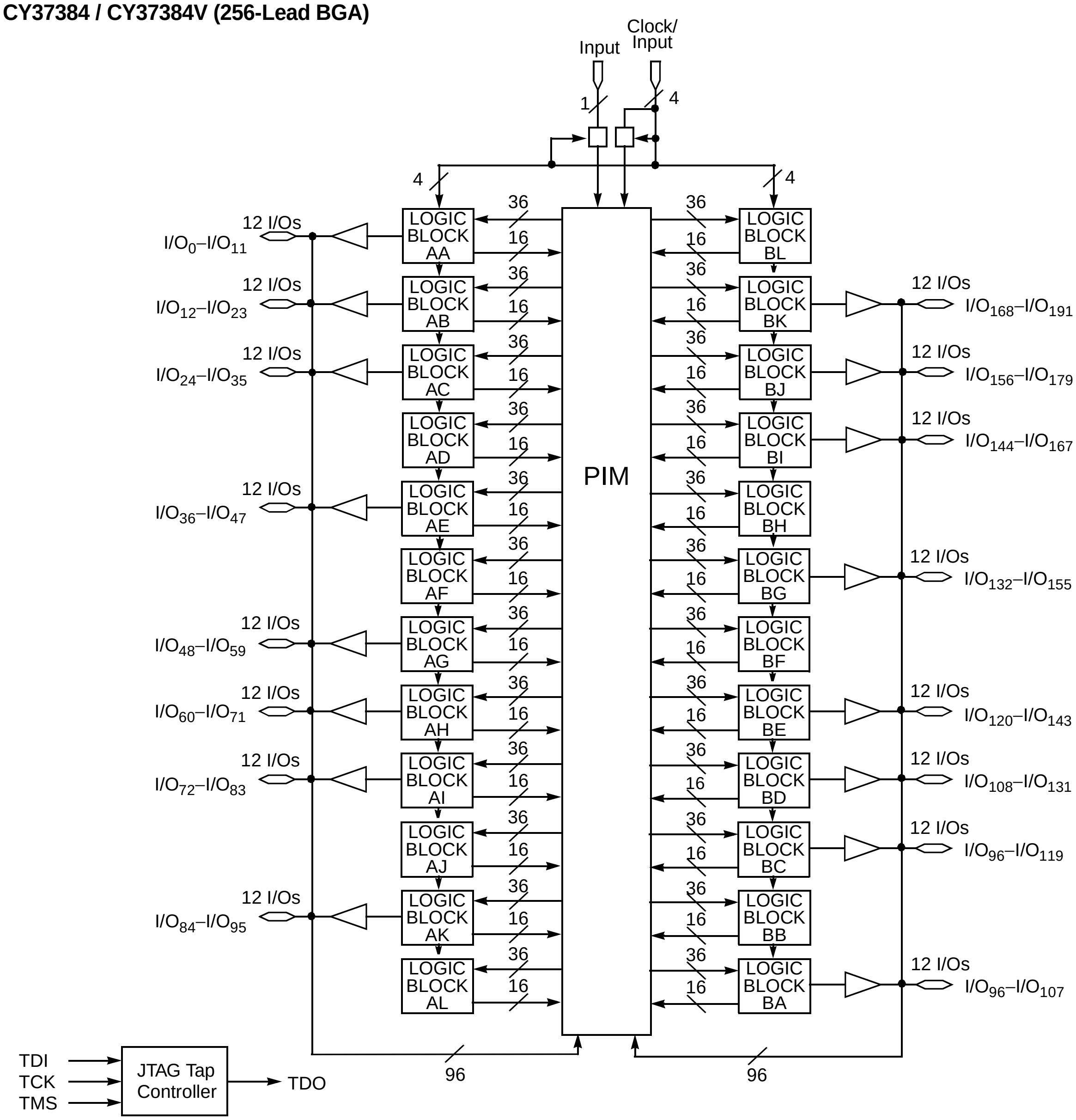
Logic Block Diagrams (continued)

CY37256 / CY37256V (256-Lead BGA)



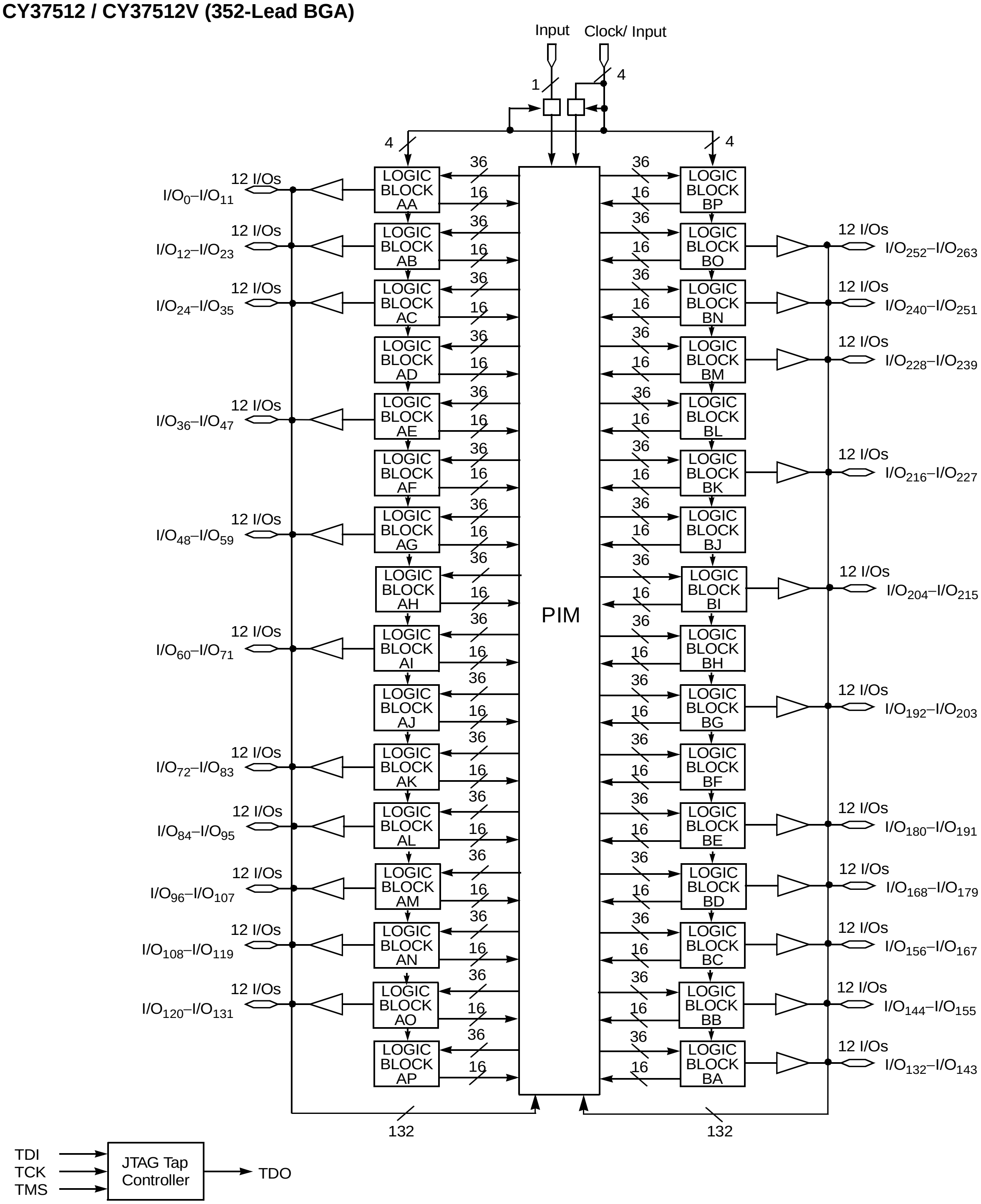
Logic Block Diagrams (continued)

CY37384 / CY37384V (256-Lead BGA)



Logic Block Diagrams (continued)

CY37512 / CY37512V (352-Lead BGA)



5.0V Device Characteristics

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with
Power Applied .... –55°C to +125°C

Supply Voltage to Ground Potential .... –0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State.. –0.5V to +7.0V

DC Input Voltage .... –0.5V to +7.0V

DC Program Voltage.. 4.5 to 5.5V

Current into Outputs .... 16 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current... >200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	Output Condition	V_{CC}	V_{CCO}
Commercial	0°C to +70°C	0°C to +90°C	5V	5V ± 0.25V	5V ± 0.25V
			3.3V	5V ± 0.25V	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V

Notes:

2. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 Family devices, please refer to the Application Note titled “An Introduction to In System Reprogramming with the Ultra37000.”
3. T_A is the “Instant On” case temperature.

5.0V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3.2 mA (Com'l/Ind)[4]	2.4			V
			I_{OH} = –2.0 mA (Mil)[4]	2.4			V
V_{OHZ}	Output HIGH Voltage with Output Disabled[5]	V_{CC} = Max.	I_{OH} = 0 µA (Com'l)[6]			4.2	V
			I_{OH} = 0 µA (Ind/Mil)[6]			4.5	V
			I_{OH} = –100 µA (Com'l)[6]			3.6	V
			I_{OH} = –150 µA (Ind/Mil)[6]			3.6	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)[4]			0.5	V
			I_{OL} = 12 mA (Mil)[4]			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0		V_{CCmax}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5		0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10		10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50		50	µA
I_{OS}	Output Short Circuit Current[8, 5]	V_{CC} = Max., V_{OUT} = 0.5V		–30		–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75			µA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75			µA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.				+500	µA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.				–500	µA

Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	10	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual Function Pins[9]	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

Notes:

4. I_{OH} = –2 mA, I_{OL} = 2 mA for TDO.
5. Tested initially and after any design or process changes that may affect these parameters.
6. When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to above 3.6V if no leakage current is allowed. Note that all I/Os are output disabled during ISR programming. Refer to the application note "Understanding Bus-Hold" for additional information.
7. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
8. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
9. Dual pins are I/O with JTAG pins.

3.3V Device Characteristics

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied ....–55°C to +125°C

Supply Voltage to Ground Potential .... –0.5V to +4.6V

DC Voltage Applied to Outputs
in High Z State...–0.5V to +7.0V

DC Input Voltage ....–0.5V to +7.0V

DC Program Voltage.. 3.0 to 3.6V

Current into Outputs .... 8 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current.. >200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	3.3V ± 0.3V

3.3V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –4 mA (Com'l)[4]	2.4		V
			I_{OH} = –3 mA (Mil)[4]			
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8 mA (Com'l)[4]		0.5	V
			I_{OL} = 6 mA (Mil)[4]			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5	0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10	10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50	50	µA
I_{OS}	Output Short Circuit Current[8, 5]	V_{CC} = Max., V_{OUT} = 0.5V		–30	–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75		µA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75		µA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.			+500	µA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.			–500	µA

Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 3.3V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

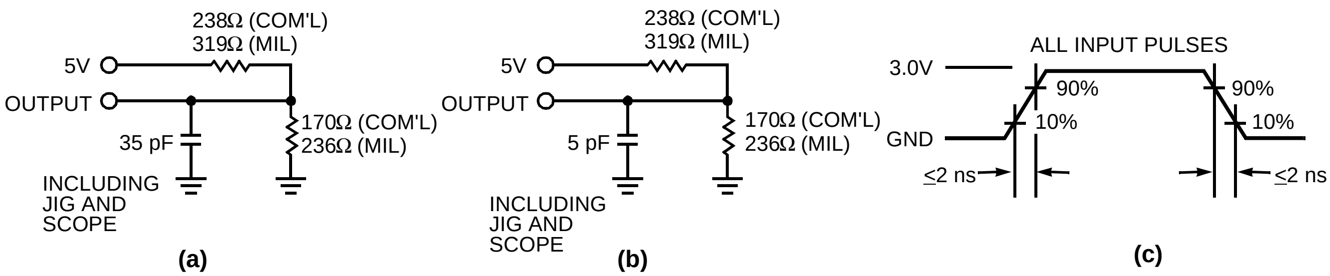
Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual Functional Pins[9]	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

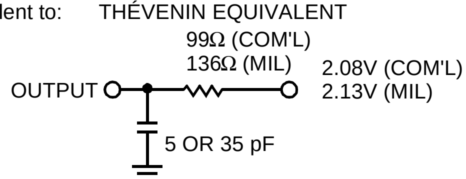
Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

AC Characteristics.

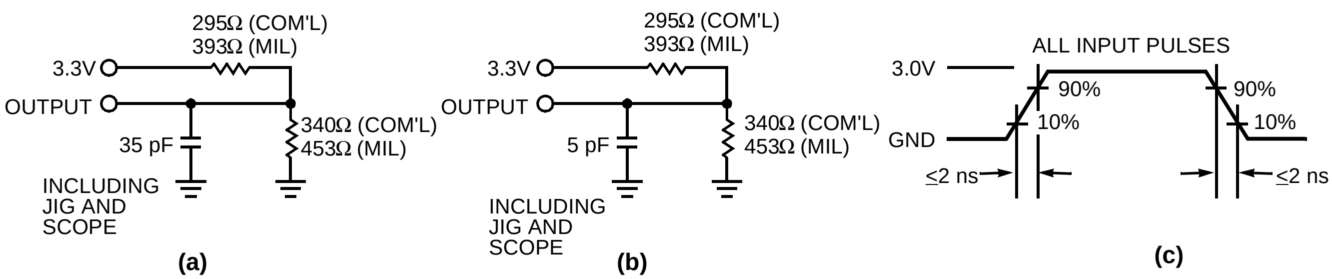
5.0V AC Test Loads and Waveforms



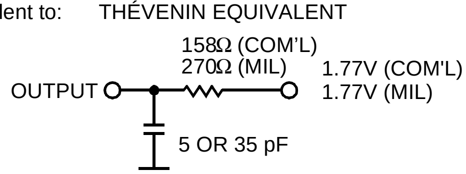
Equivalent to: THÉVENIN EQUIVALENT

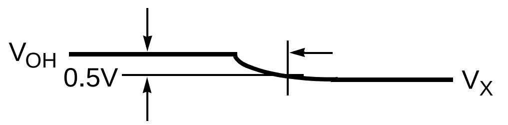
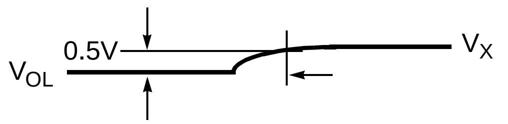
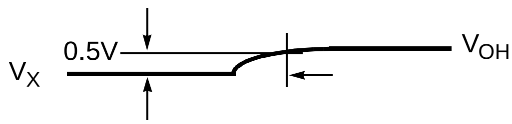
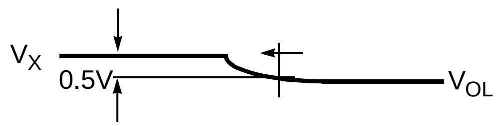


3.3V AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameter[10]	**V_X**	**Output Waveform—Measurement Level**
$t_{ER(–)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(–)}$	V_{the}	

(d) Test Waveforms

Note:

10. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.

Switching Characteristics Over the Operating Range[11]

Parameter	Description	Unit
Combinatorial Mode Parameters		
t_{PD}[12, 13, 14]	Input to Combinatorial Output	ns
t_{PDL}[12, 13, 14]	Input to Output Through Transparent Input or Output Latch	ns
t_{PDLL}[12, 13, 14]	Input to Output Through Transparent Input and Output Latches	ns
t_{EA}[12, 13, 14]	Input to Output Enable	ns
t_{ER}[10, 12]	Input to Output Disable	ns
Input Register Parameters		
t_{WL}	Clock or Latch Enable Input LOW Time[8]	ns
t_{WH}	Clock or Latch Enable Input HIGH Time[8]	ns
t_{IS}	Input Register or Latch Set-Up Time	ns
t_{IH}	Input Register or Latch Hold Time	ns
t_{ICO}[12, 13, 14]	Input Register Clock or Latch Enable to Combinatorial Output	ns
t_{ICOL}[12, 13, 14]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch	ns
Synchronous Clocking Parameters		
t_{CO}[13, 14]	Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output	ns
t_S[12]	Set-Up Time from Input to Sync. Clk (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
t_H	Register or Latch Data Hold Time	ns
t_{CO2}[12, 13, 14]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Combinatorial Output Delay (Through Logic Array)	ns
t_{SCS}[12]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable (Through Logic Array)	ns
t_{SL}[12]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK_0 CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
Product Term Clocking Parameters		
t_{COPT}[12, 13, 14]	Product Term Clock or Latch Enable (PTCLK) to Output	ns
t_{SPT}	Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK)	ns
t_{HPT}	Register or Latch Data Hold Time	ns
t_{ISPT}[12]	Set-Up Time for Buried Register used as an Input Register from Input to Product Term Clock or Latch Enable (PTCLK)	ns
t_{IHPT}	Buried Register Used as an Input Register or Latch Data Hold Time	ns
t_{CO2PT}[12, 13, 14]	Product Term Clock or Latch Enable (PTCLK) to Output Delay (Through Logic Array)	ns
Pipelined Mode Parameters		
t_{ICS}[12]	Input Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) to Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3)	ns

Notes:

11. All AC parameters are measured with two outputs switching and 35-pF AC Test Load.
12. Logic Blocks operating in Low-Power Mode, add t_{LP} to this spec.
13. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.
14. When V_{CCO}= 3.3V, add $t_{3.3IO}$ to this spec.

Switching Characteristics Over the Operating Range[11] (continued)

Parameter	Description	Unit
Operating Frequency Parameters		
f_{MAX1}	Maximum Frequency with Internal Feedback (Lesser of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$)[5]	MHz
f_{MAX4}	Maximum Frequency in Pipelined Mode (Lesser of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)[5]	MHz
Reset/Preset Parameters		
t_{RW}	Asynchronous Reset Width[5]	ns
t_{RR}[12]	Asynchronous Reset Recovery Time[5]	ns
t_{RO}[12, 13, 14]	Asynchronous Reset to Output	ns
t_{PW}	Asynchronous Preset Width[5]	ns
t_{PR}[12]	Asynchronous Preset Recovery Time[5]	ns
t_{PO}[12, 13, 14]	Asynchronous Preset to Output	ns
User Option Parameters		
t_{LP}	Low Power Adder	ns
t_{SLEW}	Slow Output Slew Rate Adder	ns
$t_{3.3IO}$	3.3V I/O Mode Timing Adder[5]	ns
JTAG Timing Parameters		
$t_{S\ JTAG}$	Set-Up Time from TDI and TMS to TCK[5]	ns
$t_{H\ JTAG}$	Hold Time on TDI and TMS[5]	ns
$t_{CO\ JTAG}$	Falling Edge of TCK to TDO[5]	ns
f_{JTAG}	Maximum JTAG Tap Controller Frequency[5]	ns

Switching Characteristics Over the Operating Range[11]

Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters																	
t_{PD}[12, 13, 14]		6		6.5		7.5		8.5		10		12		15		20	ns
t_{PDL}[12, 13, 14]		11		12.5		14.5		16		16.5		17		19		22	ns
t_{PDLL}[12, 13, 14]		12		13.5		15.5		17		17.5		18		20		24	ns
t_{EA}[12, 13, 14]		8		8.5		11		13		14		16		19		24	ns
t_{ER}[10, 12]		8		8.5		11		13		14		16		19		24	ns
Input Register Parameters																	
t_{WL}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t_{WH}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t_{IS}	2		2		2		2		2		2.5		3		4		ns
t_{IH}	2		2		2		2		2		2.5		3		4		ns
t_{ICO}[12, 13, 14]		11		11		11		12.5		12.5		16		19		24	ns
t_{ICOL}[12, 13, 14]		12		12		12		14		16		18		21		26	ns
Synchronous Clocking Parameters																	
t_{CO} [13, 14]		4		4		4.5		6		6.5[15]		6.5[16]		8[17]		10	ns
t_S[12]	4		4		5		5		5.5[15]		6[16]		8[17]		10		ns
t_H	0		0		0		0		0		0		0		0		ns
t_{CO2}[12, 13, 14]		9.5		10		11		12		14		16		19		24	ns
t_{SCS}[12]	5		6		6.5		7		8[15]		10		12		15		ns
t_{SL}[12]	7.5		7.5		8.5		9		10		12		15		15		ns
t_{HL}	0		0		0		0		0		0		0		0		ns
Product Term Clocking Parameters																	
t_{COPT}[12, 13, 14]		7		10		10		13		13		13		15		20	ns
t_{SPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t_{HPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t_{ISPT}[12]	0		0		0		0		0		0		0		0		ns
t_{IHPT}	6		6.5		6.5		7.5		9		11		14		19		ns
t_{CO2PT}[12, 13, 14]		12		14		15		19		19		21		24		30	ns
Pipelined Mode Parameters																	
t_{ICS}[12]	5		6		6		7		8[15]		10		12		15		ns
Operating Frequency Parameters																	
f_{MAX1}	200		167		154		143		125[15]		100		83		66		MHz
f_{MAX2}	200		200		200		167		154		153[16]		125[17]		100		MHz
f_{MAX3}	125		125		105		91		83		80[16]		62.5		50		MHz
f_{MAX4}	167		167		154		125		118		100		83		66		MHz

Notes:

15. The following values correspond to the CY37512 and CY37384 devices: t_{CO} = 5 ns, t_S = 6.5 ns, t_{SCS} = 8.5 ns, t_{ICS} = 8.5 ns, f_{MAX1} = 118 MHz.
16. The following values correspond to the CY37192V and CY37256V devices: t_{CO} = 6 ns, t_S = 7 ns, f_{MAX2} = 143 MHz, f_{MAX3} = 77 MHz, and f_{MAX4} = 100 MHz; and for the CY37512 devices: t_S = 7 ns.
17. The following values correspond to the CY37512V and CY37384V devices: t_{CO} = 6.5 ns, t_S = 9.5 ns, and f_{MAX2} = 105 MHz.

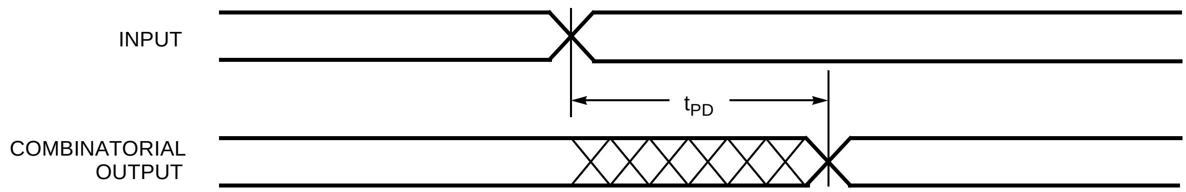
Switching Characteristics Over the Operating Range[11] (continued)

Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters																	
t_{RW}	8		8		8		8		10		12		15		20		ns
t_{RR}[12]	10		10		10		10		12		14		17		22		ns
t_{RO}[12, 13, 14]		12		13		13		14		15		18		21		26	ns
t_{PW}	8		8		8		8		10		12		15		20		ns
t_{PR}[12]	10		10		10		10		12		14		17		22		ns
t_{PO}[12, 13, 14]		12		13		13		14		15		18		21		26	ns
User Option Parameters																	
t_{LP}		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{SLEW}		3		3		3		3		3		3		3		3	ns
$t_{3.3IO}$[18]		0.3		0.3		0.3		0.3		0.3		0.3		0.3		0.3	ns
JTAG Timing Parameters																	
$t_{S\ JTAG}$	0		0		0		0		0		0		0		0		ns
$t_{H\ JTAG}$	20		20		20		20		20		20		20		20		ns
$t_{CO\ JTAG}$		20		20		20		20		20		20		20		20	ns
f_{JTAG}		20		20		20		20		20		20		20		20	MHz

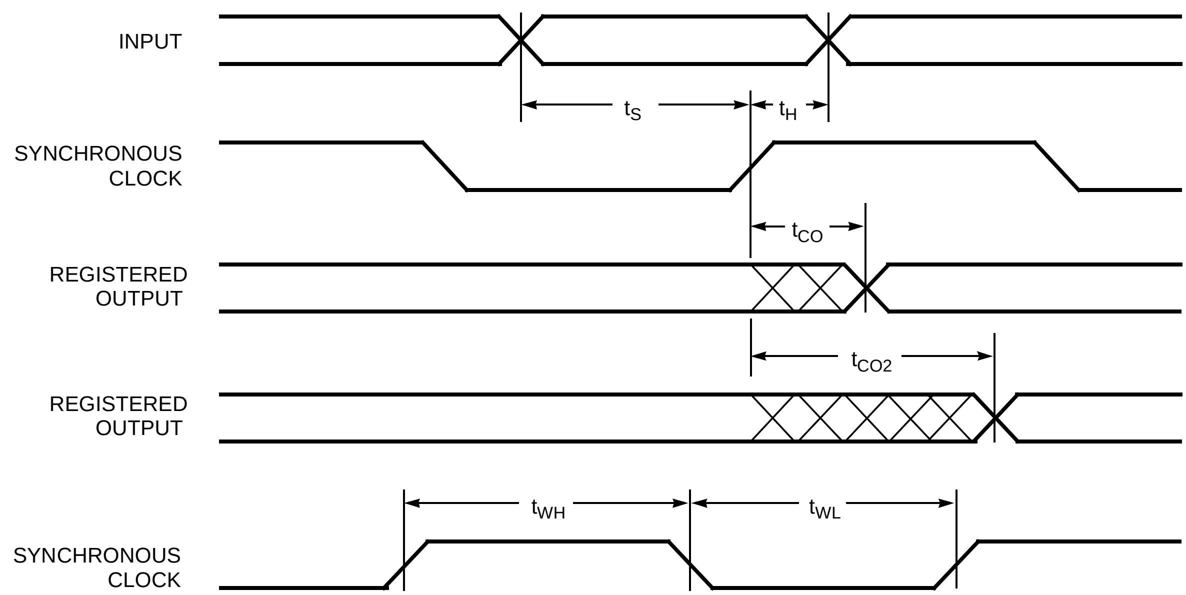
Note:
18. Only applicable to the 5V devices.

Switching Waveforms

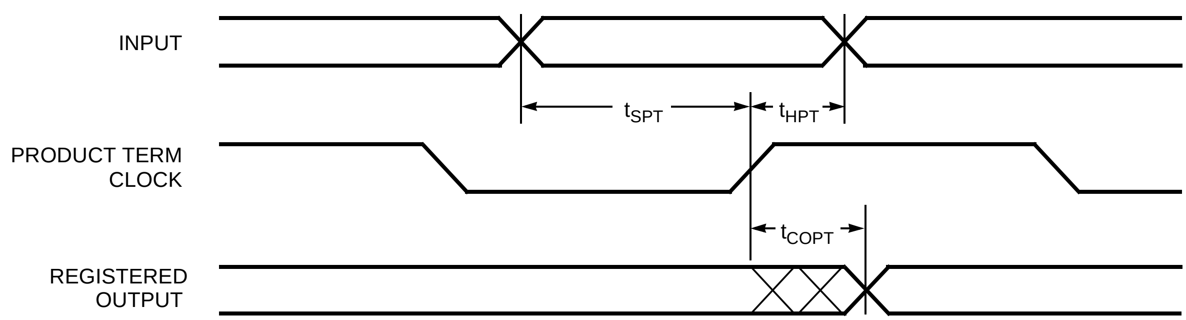
Combinatorial Output



Registered Output with Synchronous Clocking

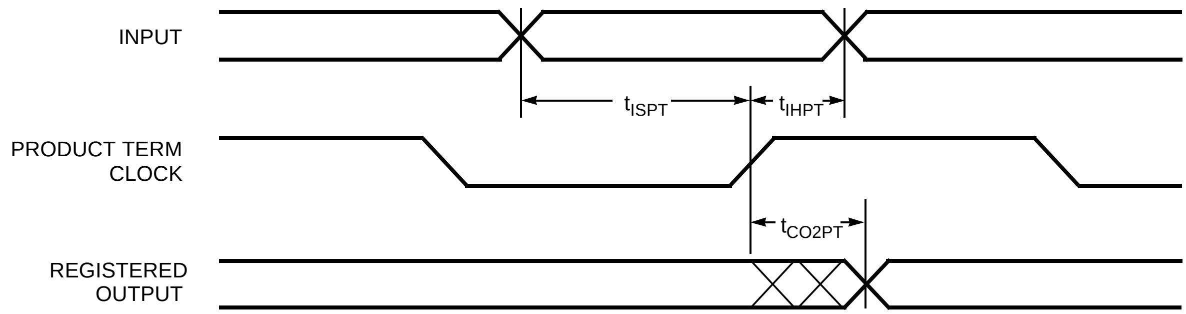


Registered Output with Product Term Clocking Input Going Through the Array

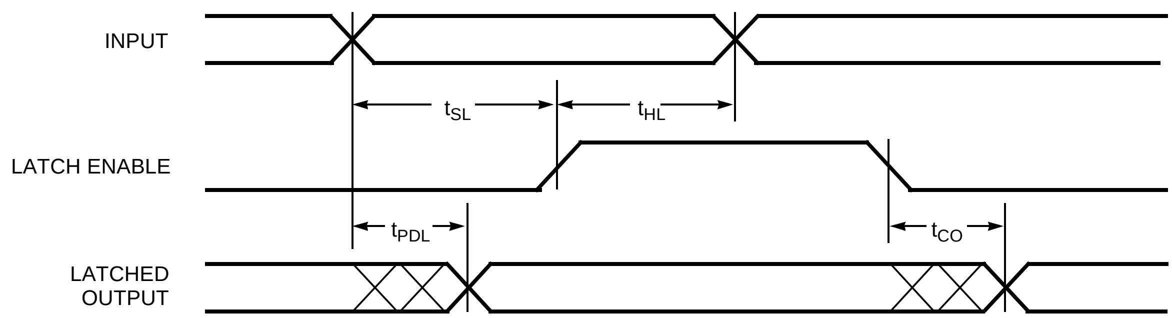


Switching Waveforms (continued)

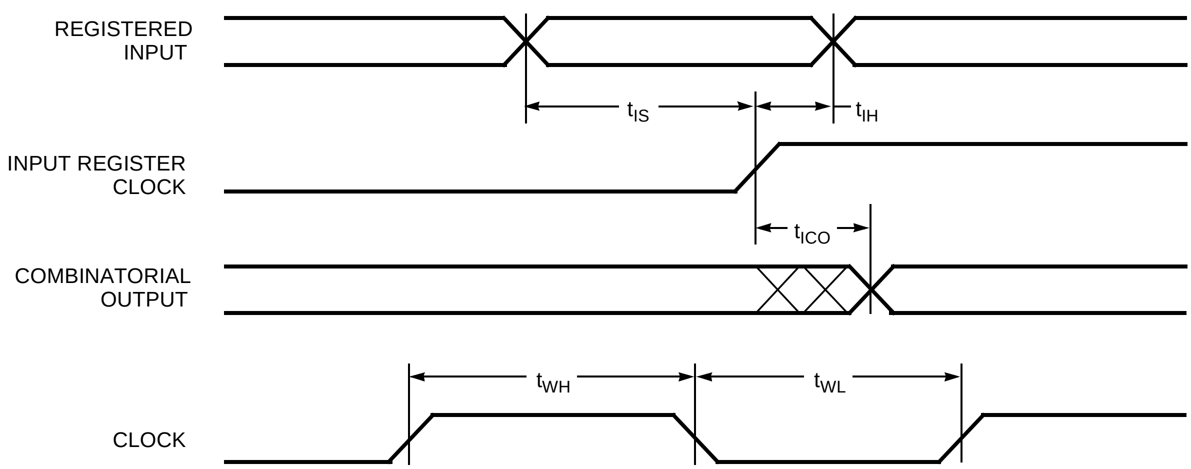
Registered Output with Product Term Clocking
Input Coming From Adjacent Buried Register



Latched Output

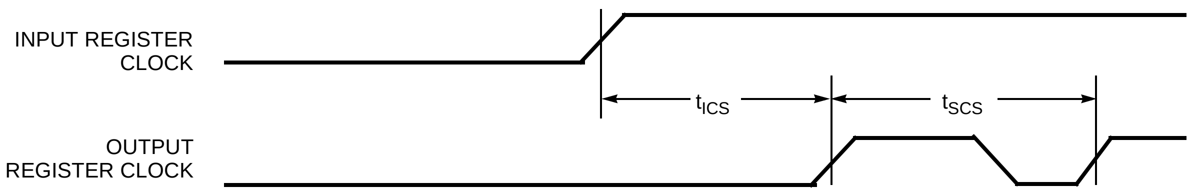


Registered Input

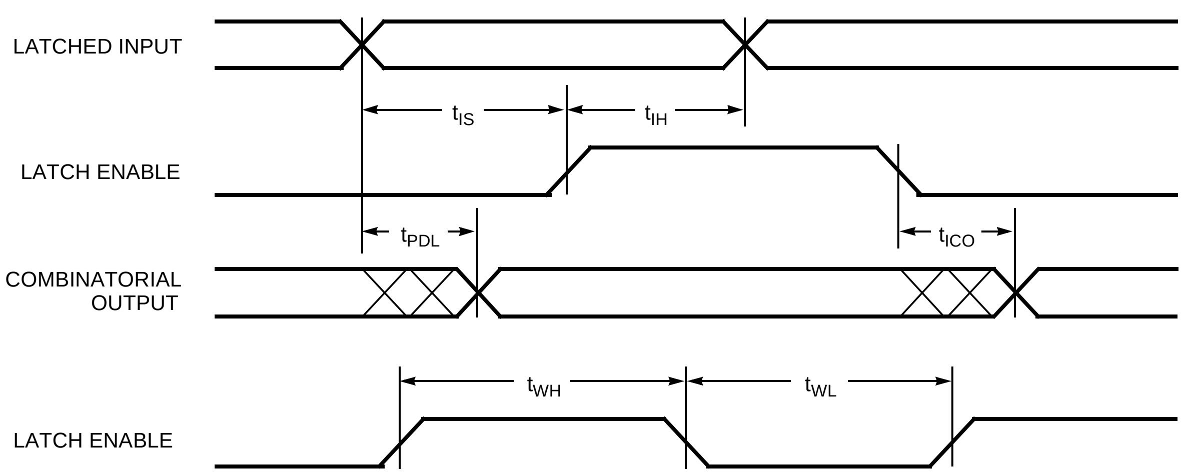


Switching Waveforms (continued)

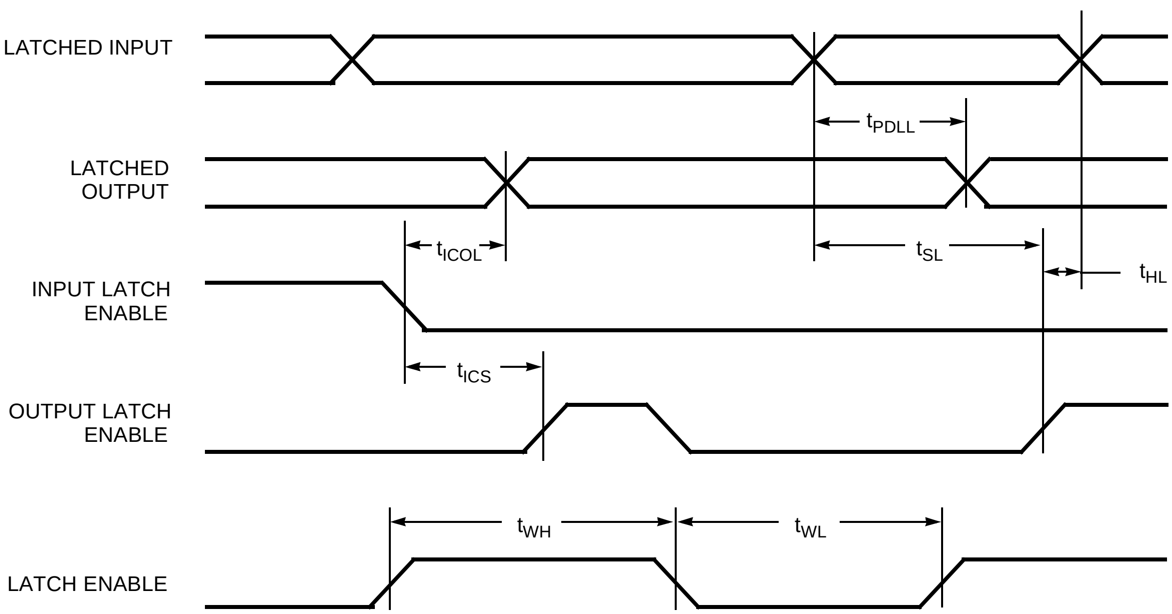
Clock to Clock



Latched Input

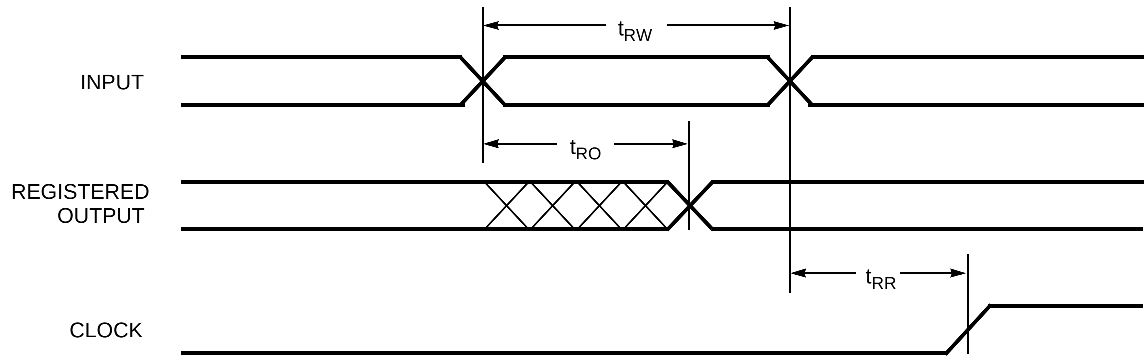


Latched Input and Output

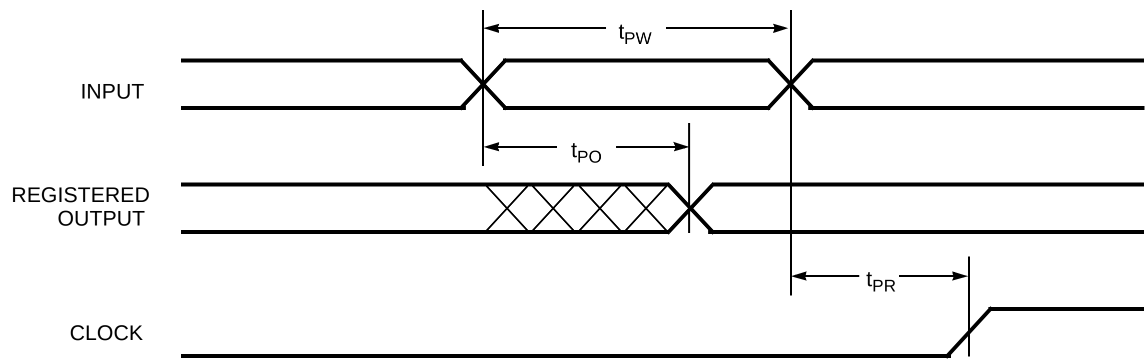


Switching Waveforms (continued)

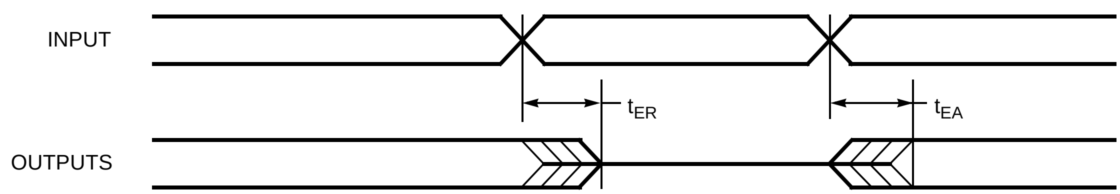
Asynchronous Reset



Asynchronous Preset



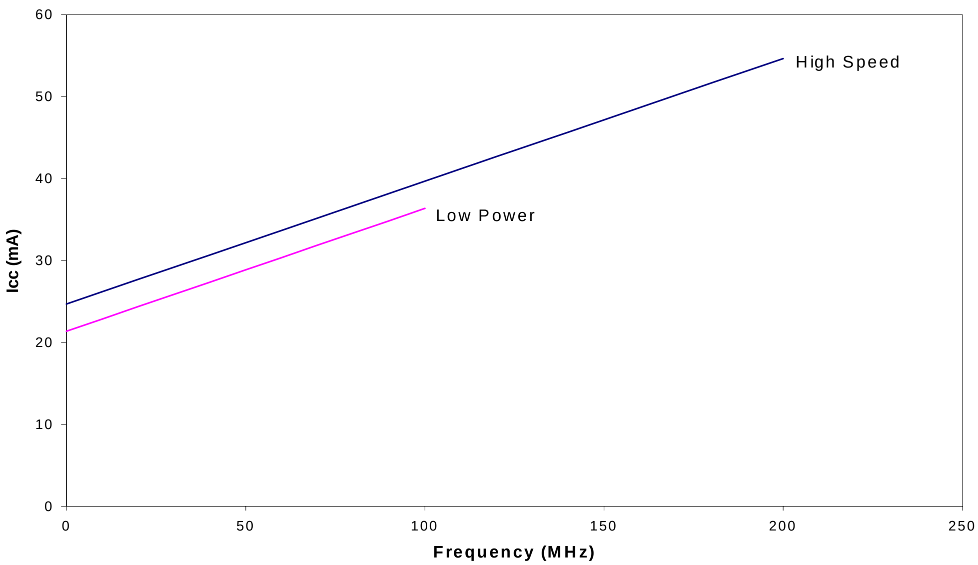
Output Enable/Disable



Power Consumption

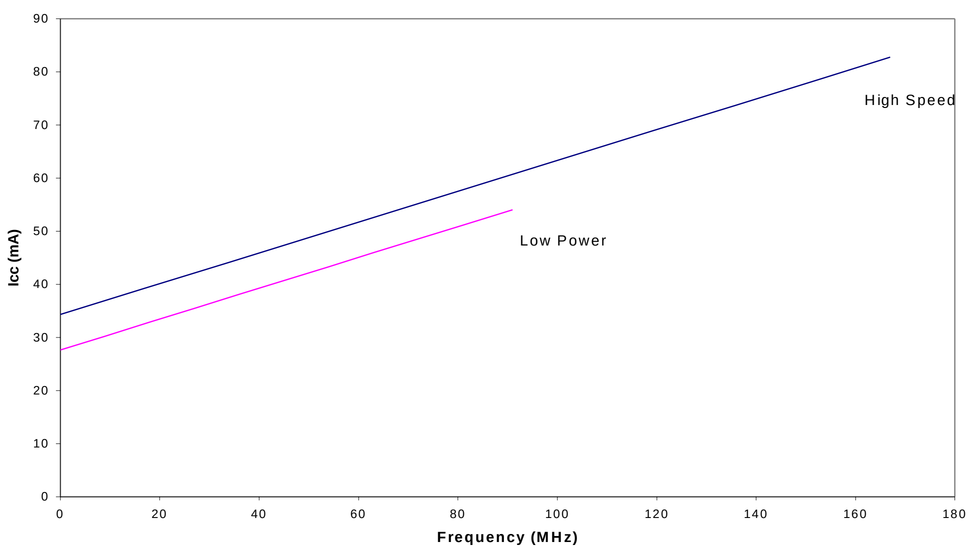
Typical 5.0V Power Consumption

CY37032



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

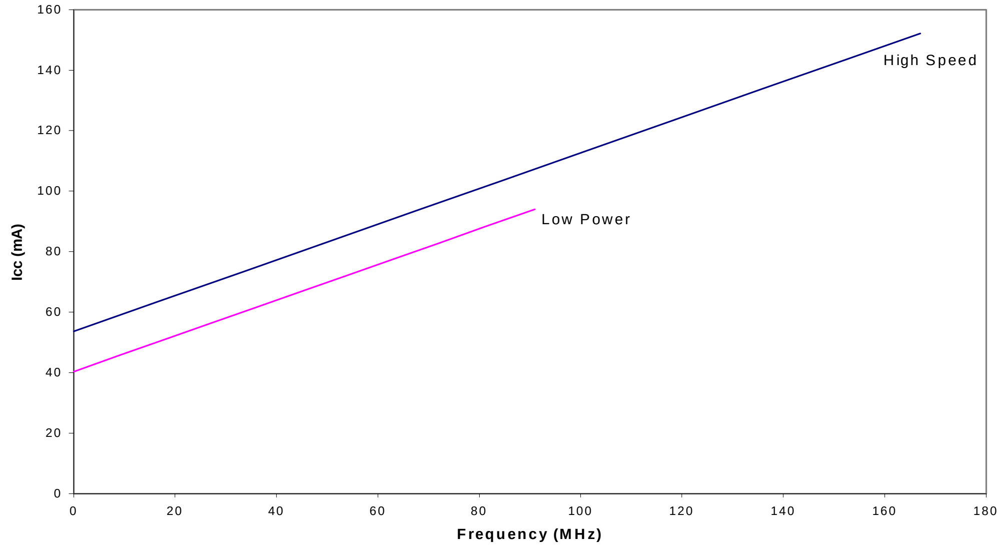
CY37064



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

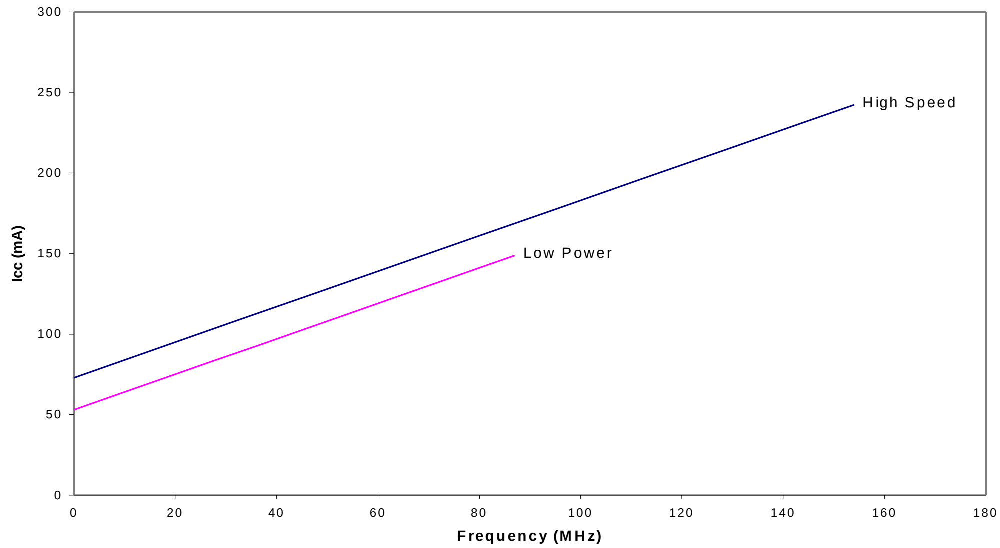
Typical 5.0V Power Consumption (continued)

CY37128



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

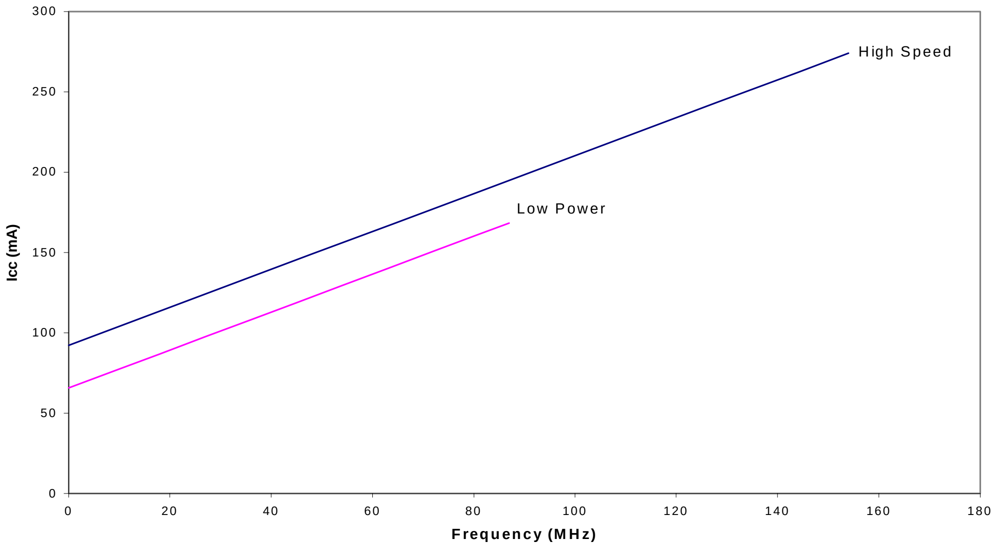
CY37192



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

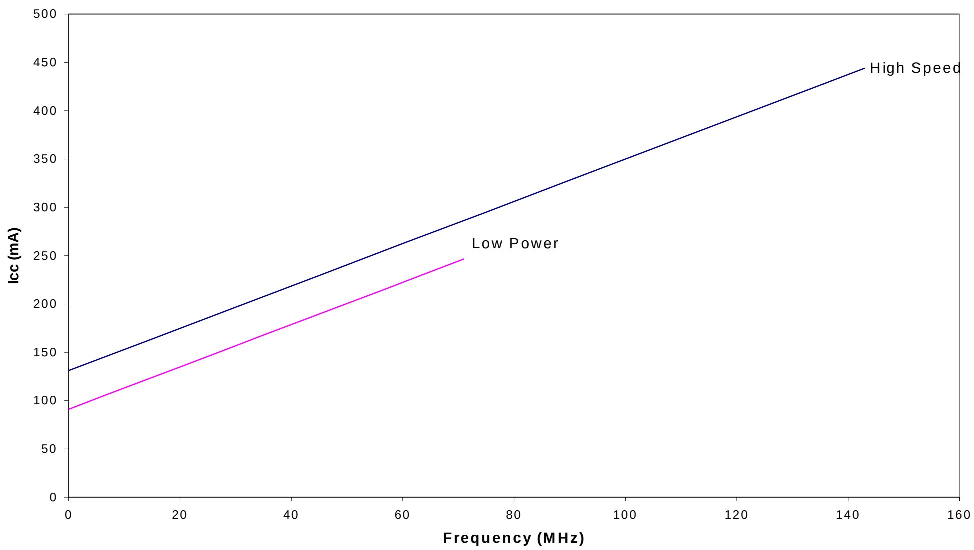
Typical 5.0V Power Consumption (continued)

CY37256



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

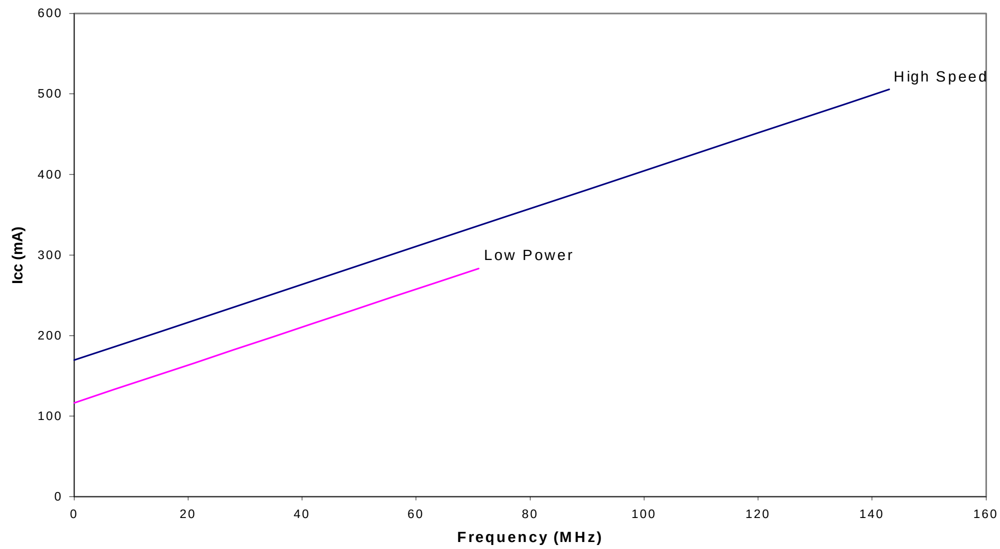
CY37384



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

Typical 5.0V Power Consumption (continued)

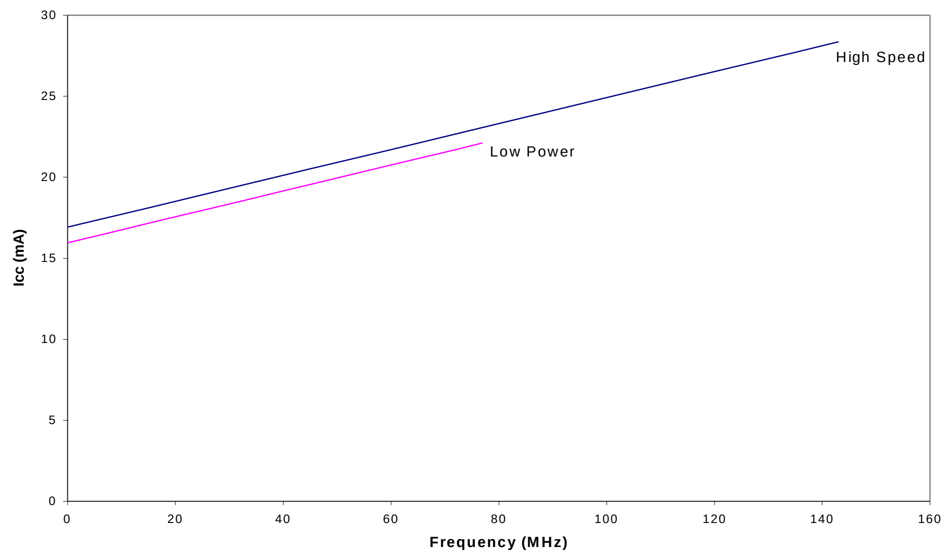
CY37512



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

Typical 3.3V Power Consumption

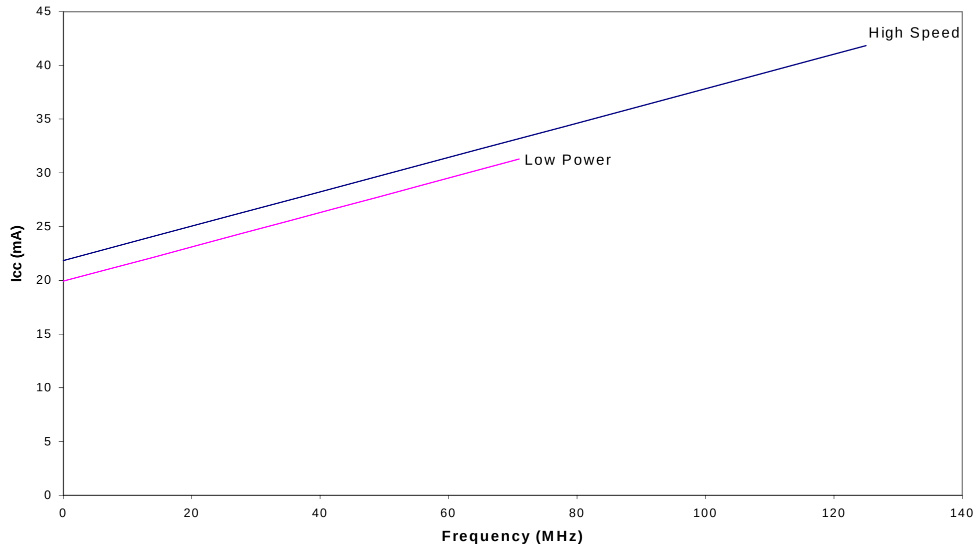
CY37032V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

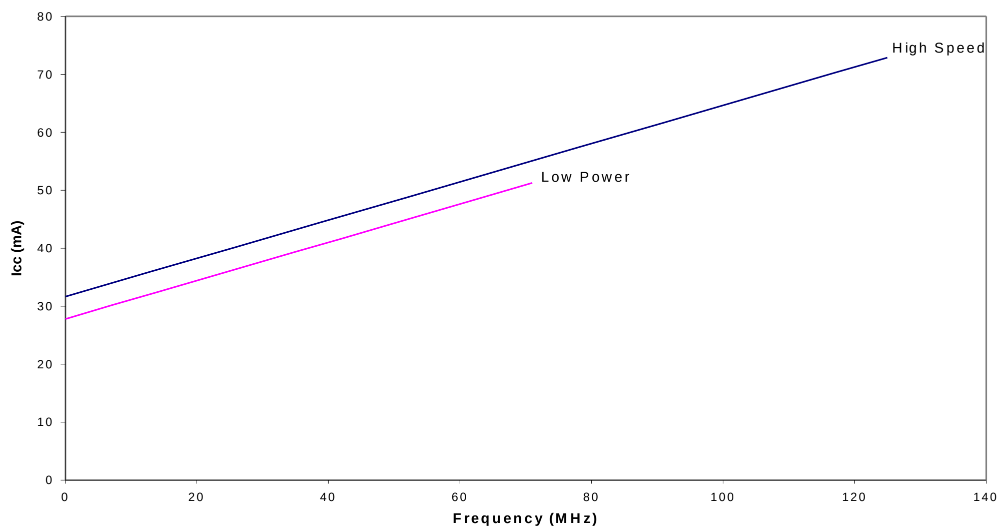
Typical 3.3V Power Consumption (continued)

CY37064V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

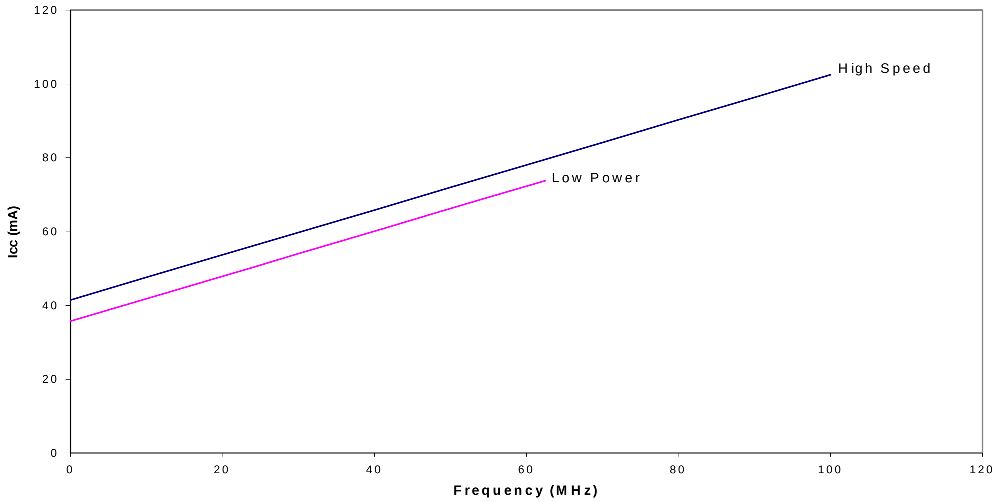
CY37128V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

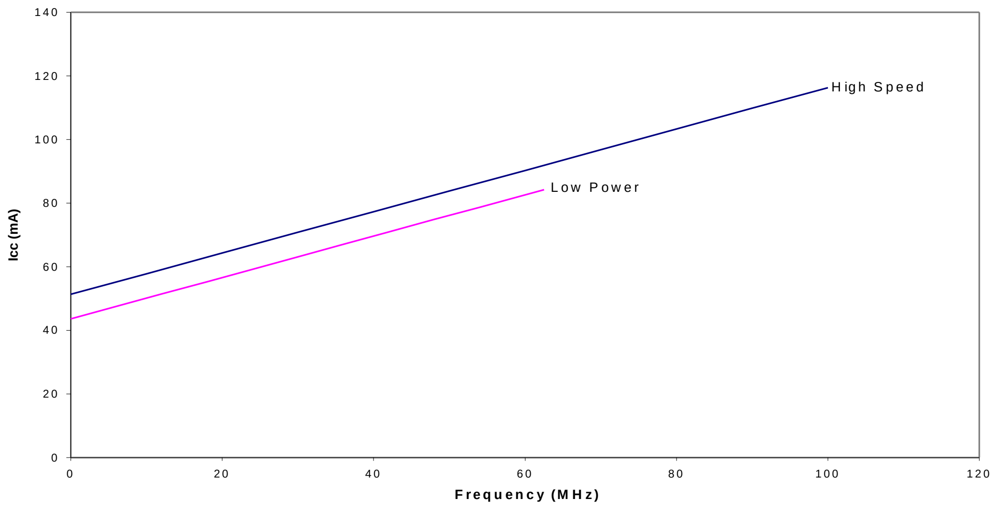
Typical 3.3V Power Consumption (continued)

CY37192V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

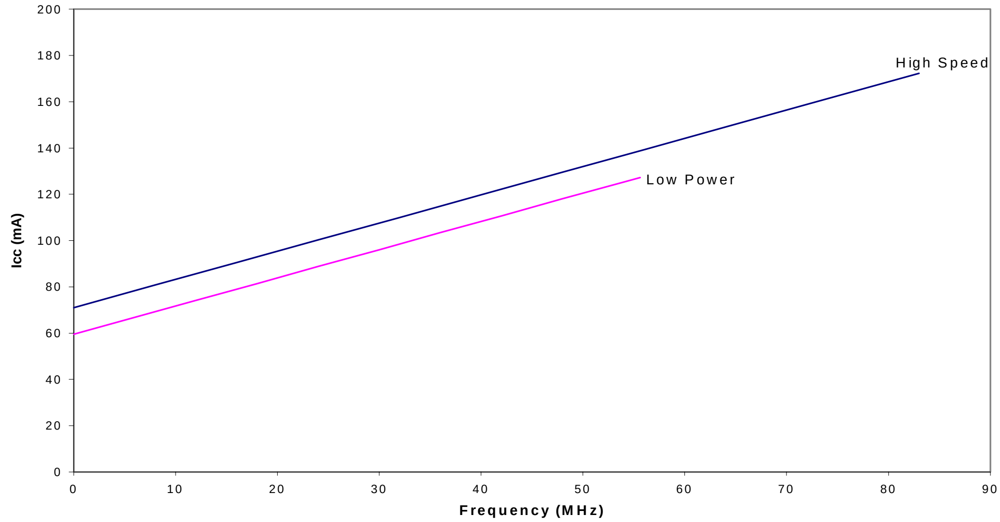
CY37256V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

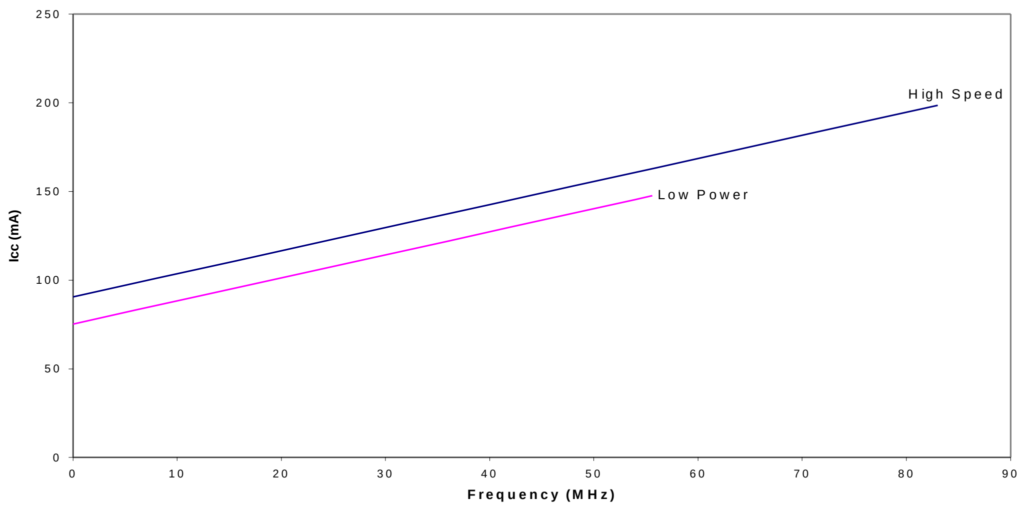
Typical 3.3V Power Consumption (continued)

CY37384V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

CY37512V

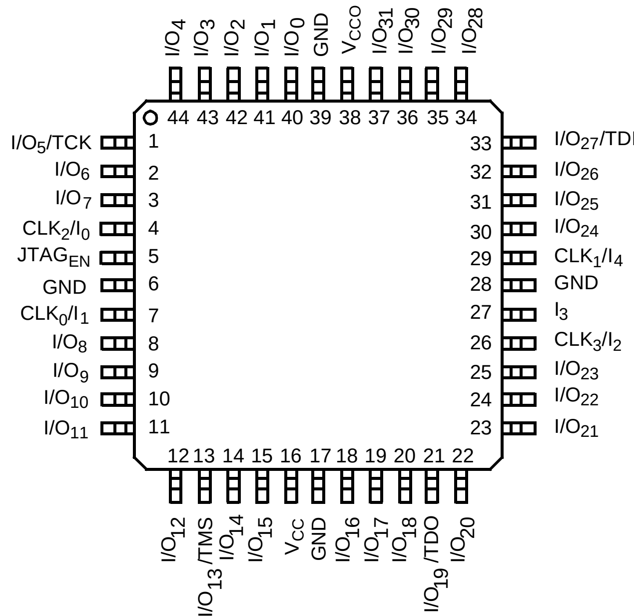


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

Pin Configurations[19]

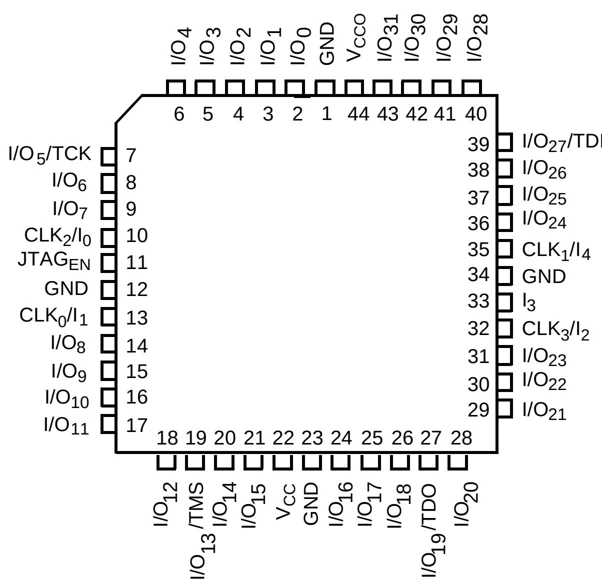
44-Pin TQFP (A44)

Top View



44-Pin PLCC (J67) / CLCC (Y67)

Top View



Note:

19. For 3.3V versions (Ultra37000V), $V_{CCO} = V_{CC}$.

Pin Configurations[19] (continued)

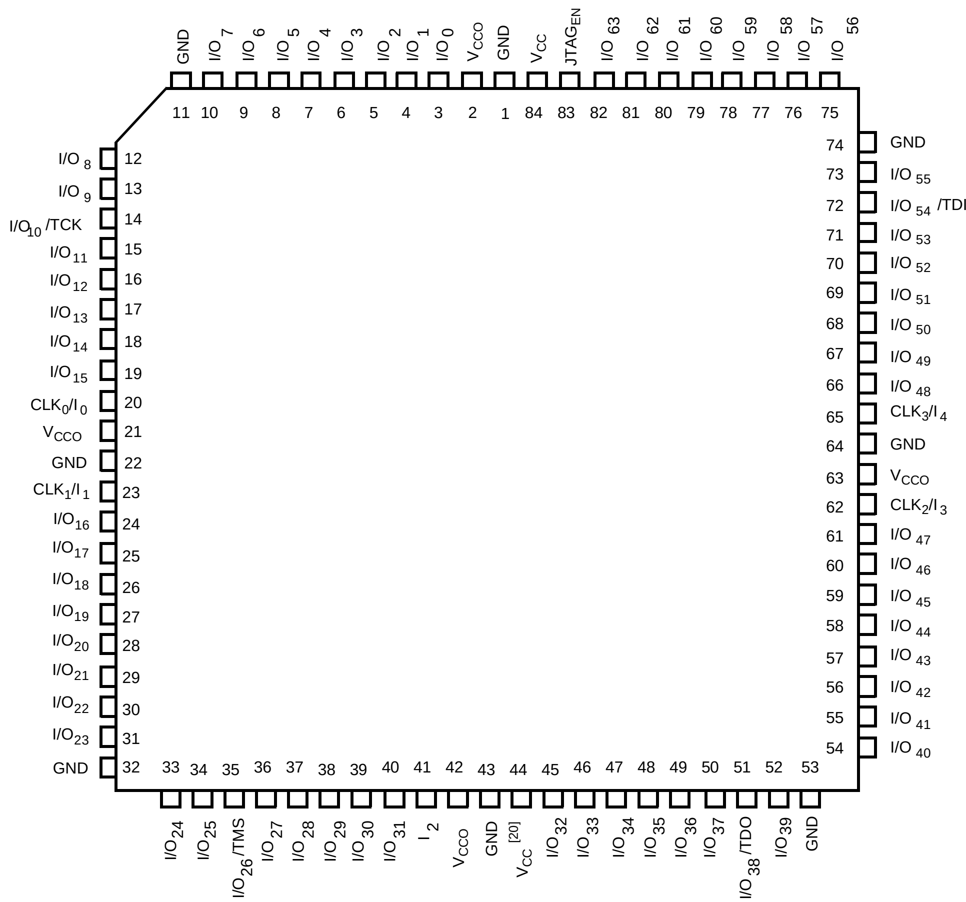
48-Ball Fine-Pitch BGA (BA50)
Top View

	1	2	3	4	5	6	7	8
A	I/O_5 TCK	V_{CC}	I/O_3	I/O_1	I/O_{31}	I/O_{30}	V_{CC}	I/O_{27} TDI
B	V_{CC}	I/O_4	I/O_2	I/O_0	I/O_{29}	I/O_{28}	I/O_{26}	CLK_1/ I_4
C	CLK_2/ I_0	I/O_7	I/O_6	GND	GND	I/O_{25}	I/O_{24}	I_3
D	$JTAG_{EN}$	I/O_8	I/O_9	GND	GND	I/O_{22}	I/O_{23}	CLK_3/ I_2
E	CLK_0/ I_1	I/O_{12}	I/O_{11}	I/O_{10}	I/O_{16}	I/O_{20}	I/O_{21}	V_{CC}
F	I/O_{13} TMS	V_{CC}	I/O_{14}	I/O_{15}	I/O_{17}	I/O_{18}	V_{CC}	I/O_{19} TDO

Pin Configurations[19] (continued)

84-Lead PLCC (J83) / CLCC (Y84)

Top View

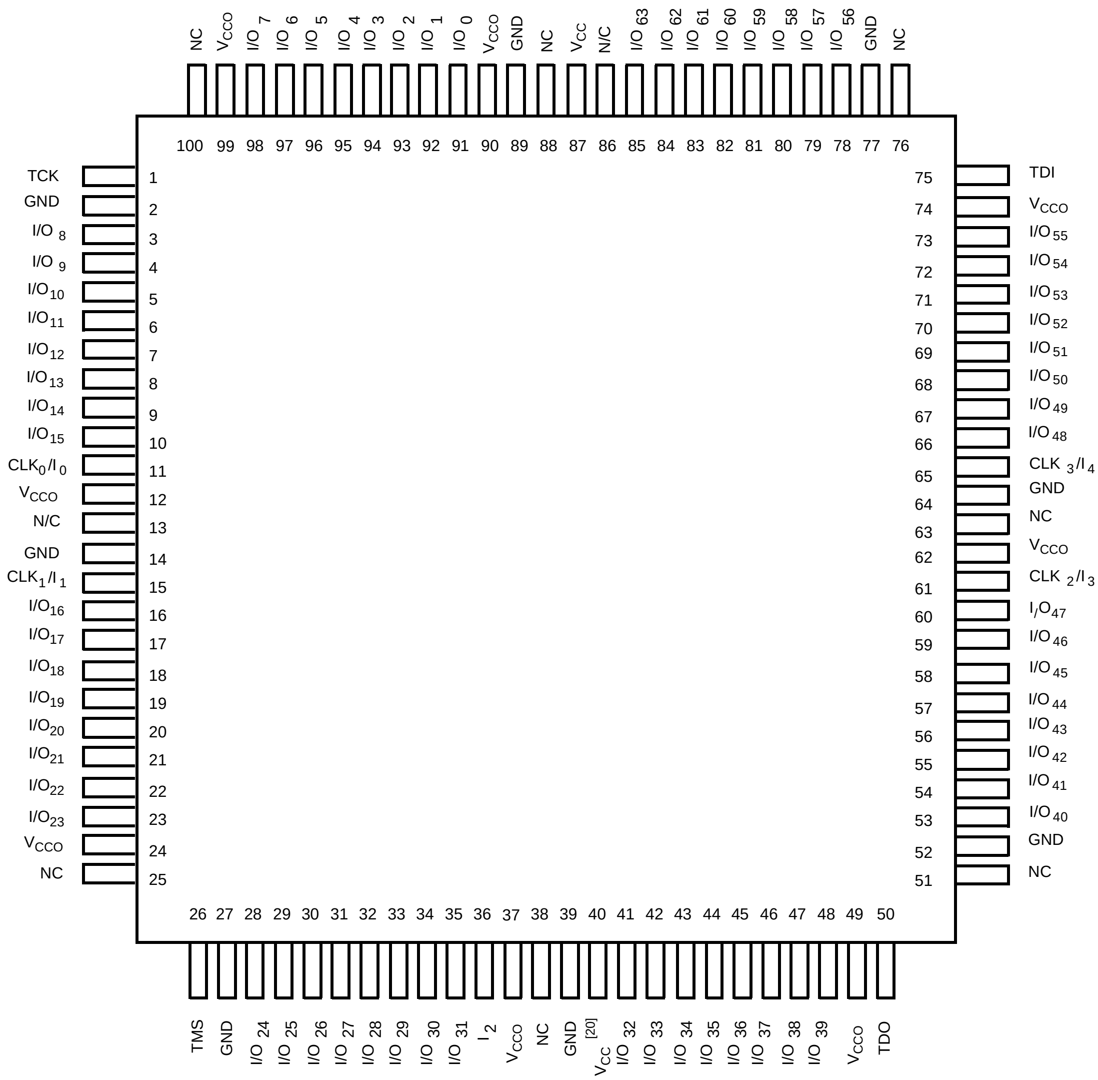


Note:

20. This pin is a N/C, but Cypress recommends that you connect it to V_{CC} to ensure future compatibility.

Pin Configurations[19] (continued)

100-Lead TQFP (A100)
Top View



Pin Configurations[19] (continued)

100-Ball Fine-Pitch BGA (BB100) for CY37064V Top View

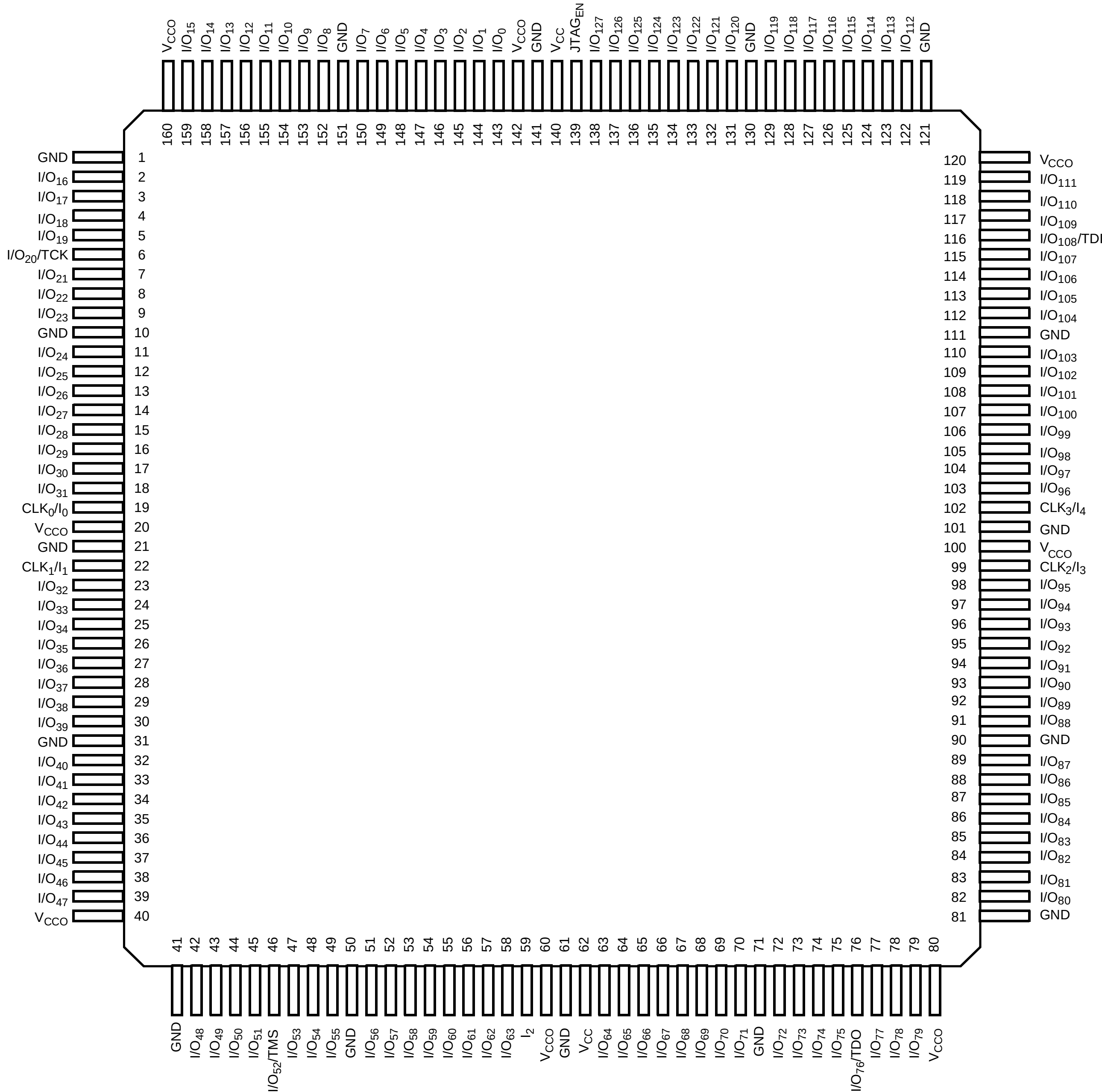
	1	2	3	4	5	6	7	8	9	10
A	NC	NC	I/O_7	I/O_5	I/O_2	I/O_{62}	I/O_{60}	I/O_{58}	I/O_{57}	I/O_{56}
B	I/O_9	I/O_8	I/O_6	I/O_4	I/O_1	I/O_{63}	V_{CC}	I/O_{59}	I/O_{55}	NC
C	I/O_{10}	TCK	V_{CC}	I/O_3	NC	NC	I/O_{61}	V_{CC}	TDI	I/O_{54}
D	I/O_{11}	NC	I/O_{12}	I/O_{13}	I/O_0	NC	I/O_{51}	I/O_{52}	CLK_3/I_4	I/O_{53}
E	I/O_{14}	CLK_0/I_0	I/O_{15}	NC	GND	GND	I/O_{48}	I/O_{49}	CLK_2/I_3	I/O_{50}
F	I/O_{17}	NC	NC	I/O_{16}	GND	GND	NC	NC	I_2	I/O_{47}
G	I/O_{22}	CLK_1/I_1	I/O_{21}	I/O_{19}	I/O_{18}	I/O_{46}	I/O_{45}	I/O_{44}	NC	I/O_{43}
H	I/O_{23}	TMS	V_{CC}	I/O_{20}	NC	I/O_{32}	I/O_{42}	V_{CC}	TDO	I/O_{41}
J	NC	I/O_{26}	I/O_{28}	NC	I/O_{31}	I/O_{33}	I/O_{35}	I/O_{37}	I/O_{39}	I/O_{40}
K	I/O_{24}	I/O_{25}	I/O_{27}	I/O_{29}	I/O_{30}	I/O_{34}	I/O_{36}	I/O_{38}	NC	NC

100-Ball Fine-Pitch BGA (BB100) for CY37128V Top View

	1	2	3	4	5	6	7	8	9	10
A	NC	I/O_9	I/O_8	I/O_6	I/O_3	I/O_{76}	I/O_{74}	I/O_{72}	I/O_{71}	I/O_{70}
B	I/O_{11}	I/O_{10}	I/O_7	I/O_5	I/O_2	I/O_{77}	V_{CC}	I/O_{73}	I/O_{68}	I/O_{69}
C	I/O_{12}	I/O_{13} TCK	V_{CC}	I/O_4	I/O_1	I/O_{78}	I/O_{75}	V_{CC}	I/O_{67} TDI	I/O_{66}
D	I/O_{14}	V_{CC}	I/O_{15}	I/O_{16}	I/O_0	I/O_{79}	I/O_{63}	I/O_{64}	CLK_3/I_4	I/O_{65}
E	I/O_{17}	CLK_0/I_0	I/O_{18}	I/O_{19}	GND	GND	I/O_{60}	I/O_{61}	CLK_2/I_3	I/O_{62}
F	I/O_{22}	$JTAG_{EN}$	I/O_{21}	I/O_{20}	GND	GND	I/O_{59}	I/O_{58}	I_2	I/O_{57}
G	I/O_{27}	CLK_1/I_1	I/O_{26}	I/O_{24}	I/O_{23}	I/O_{56}	I/O_{55}	I/O_{54}	V_{CC}	I/O_{53}
H	I/O_{28}	I/O_{33} TMS	V_{CC}	I/O_{25}	I/O_{39}	I/O_{40}	I/O_{52}	V_{CC}	I/O_{47} TDO	I/O_{51}
J	I/O_{29}	I/O_{32}	I/O_{35}	V_{CC}	I/O_{38}	I/O_{41}	I/O_{43}	I/O_{45}	I/O_{48}	I/O_{50}
K	I/O_{30}	I/O_{31}	I/O_{34}	I/O_{36}	I/O_{37}	I/O_{42}	I/O_{44}	I/O_{46}	I/O_{49}	NC

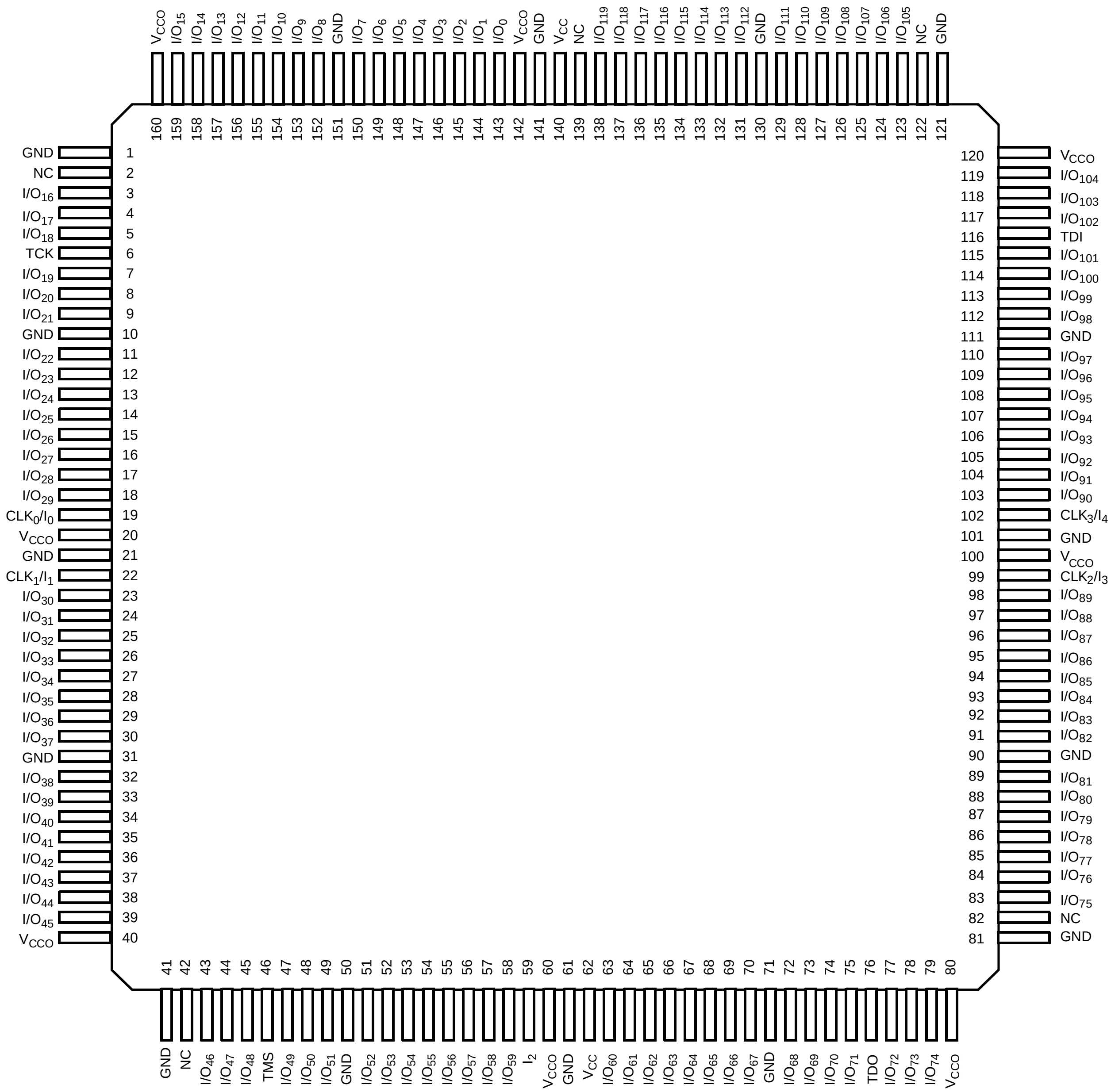
Pin Configurations[19] (continued)

160-Lead TQFP (A160) / CQFP (U162)
for CY37128(V) and CY37256(V)
Top View



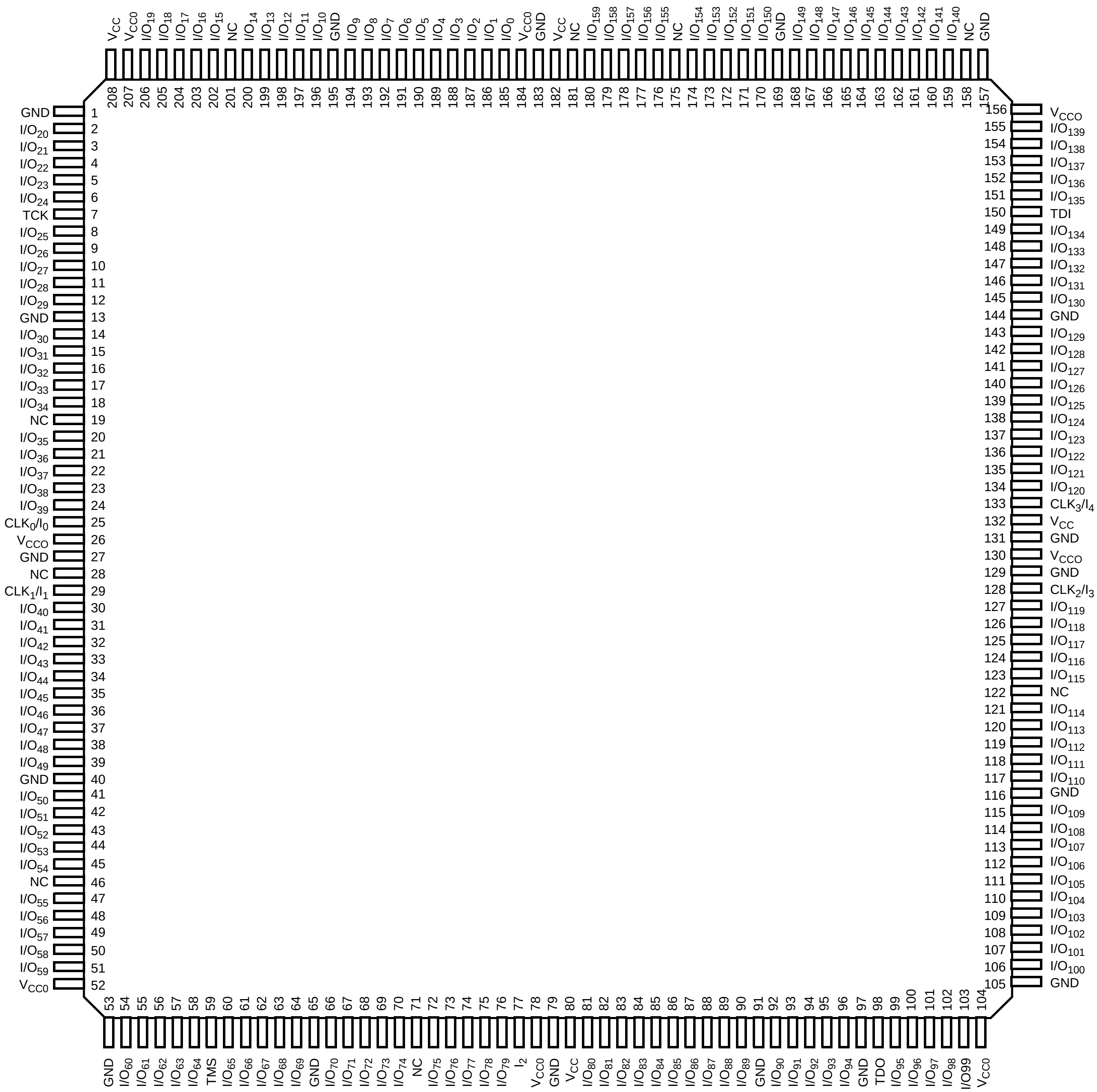
Pin Configurations[19] (continued)

160-Lead TQFP (A160) for CY37192(V)
Top View



Pin Configurations[19] (continued)

208-Lead PQFP (N208) / CQFP (U208)
Top View



Pin Configurations[19] (continued)

256-Ball PBGA (BG256)
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	I/O$_{21}$	NC	I/O$_{16}$	I/O$_{12}$	I/O$_{9}$	I/O$_{7}$	I/O$_{4}$	I/O$_{0}$	I/O$_{190}$	I/O$_{189}$	I/O$_{186}$	I/O$_{182}$	NC	I/O$_{178}$	I/O$_{175}$	NC	NC	I/O$_{169}$	I/O$_{168}$	A
B	I/O$_{23}$	I/O$_{20}$	I/O$_{19}$	I/O$_{18}$	I/O$_{15}$	I/O$_{11}$	I/O$_{8}$	I/O$_{5}$	I/O$_{1}$	I/O$_{191}$	I/O$_{187}$	I/O$_{185}$	I/O$_{181}$	NC	NC	I/O$_{174}$	I/O$_{171}$	I/O$_{170}$	NC	I/O$_{166}$	B
C	NC	NC	I/O$_{22}$	NC	I/O$_{17}$	I/O$_{14}$	I/O$_{10}$	I/O$_{6}$	I/O$_{2}$	NC	I/O$_{188}$	I/O$_{184}$	I/O$_{180}$	I/O$_{179}$	I/O$_{176}$	I/O$_{173}$	I/O$_{172}$	I/O$_{167}$	I/O$_{165}$	I/O$_{162}$	C
D	I/O$_{24}$	NC	NC	GND	NC	V$_{CCO}$	I/O$_{13}$	GND	I/O$_{3}$	NC	V$_{CC}$	I/O$_{183}$	GND	I/O$_{177}$	V$_{CCO}$	NC	GND	I/O$_{164}$	TDI	I/O$_{160}$	D
E	I/O$_{27}$	I/O$_{26}$	I/O$_{25}$	NC													I/O$_{163}$	I/O$_{161}$	I/O$_{159}$	I/O$_{156}$	E
F	I/O$_{30}$	TCK	I/O$_{28}$	V$_{CCO}$													V$_{CCO}$	I/O$_{158}$	NC	I/O$_{154}$	F
G	I/O$_{33}$	I/O$_{32}$	I/O$_{31}$	I/O$_{29}$													I/O$_{157}$	I/O$_{155}$	I/O$_{153}$	I/O$_{152}$	G
H	I/O$_{35}$	NC	I/O$_{34}$	GND				GND	GND	GND	GND	GND	GND				GND	I/O$_{151}$	I/O$_{150}$	I/O$_{149}$	H
J	I/O$_{39}$	I/O$_{38}$	I/O$_{37}$	I/O$_{36}$				GND	GND	GND	GND	GND	GND				I/O$_{148}$	I/O$_{147}$	I/O$_{146}$	I/O$_{145}$	J
K	I/O$_{42}$	I/O$_{40}$	I/O$_{41}$	V$_{CC}$				GND	GND	GND	GND	GND	GND				I/O$_{144}$	CLK$_{3}$/I$_{4}$	NC	NC	K
L	I/O$_{43}$	I/O$_{44}$	I/O$_{45}$	I/O$_{46}$				GND	GND	GND	GND	GND	GND				V$_{CC}$	CLK$_{2}$/I$_{3}$	I/O$_{143}$	NC	L
M	I/O$_{47}$	CLK$_{0}$/I$_{0}$	CLK$_{1}$/I$_{1}$	I/O$_{48}$				GND	GND	GND	GND	GND	GND				I/O$_{139}$	I/O$_{140}$	I/O$_{141}$	I/O$_{142}$	M
N	I/O$_{49}$	I/O$_{50}$	I/O$_{51}$	GND				GND	GND	GND	GND	GND	GND				GND	I/O$_{136}$	I/O$_{137}$	I/O$_{138}$	N
P	I/O$_{52}$	I/O$_{53}$	I/O$_{55}$	I/O$_{58}$													I/O$_{131}$	I/O$_{133}$	I/O$_{134}$	I/O$_{135}$	P
R	I/O$_{54}$	I/O$_{56}$	I/O$_{59}$	V$_{CCO}$													V$_{CCO}$	I/O$_{130}$	NC	I/O$_{132}$	R
T	I/O$_{57}$	I/O$_{60}$	I/O$_{62}$	I/O$_{65}$													I/O$_{124}$	I/O$_{127}$	I/O$_{128}$	I/O$_{129}$	T
U	I/O$_{61}$	I/O$_{63}$	I/O$_{66}$	GND	I/O$_{76}$	V$_{CCO}$	I/O$_{82}$	GND	I/O$_{91}$	V$_{CC}$	I/O$_{98}$	I/O$_{102}$	GND	I/O$_{112}$	V$_{CCO}$	NC	GND	I/O$_{123}$	I/O$_{122}$	I/O$_{126}$	U
V	I/O$_{64}$	I/O$_{67}$	I/O$_{69}$	I/O$_{75}$	I/O$_{78}$	I/O$_{81}$	I/O$_{85}$	I/O$_{88}$	I/O$_{92}$	I$_{2}$	I/O$_{97}$	I/O$_{101}$	I/O$_{105}$	I/O$_{109}$	I/O$_{113}$	TDO	I/O$_{114}$	I/O$_{117}$	I/O$_{121}$	I/O$_{125}$	V
W	I/O$_{68}$	I/O$_{70}$	I/O$_{72}$	I/O$_{74}$	I/O$_{79}$	I/O$_{83}$	I/O$_{86}$	I/O$_{89}$	I/O$_{93}$	I/O$_{95}$	I/O$_{96}$	I/O$_{100}$	I/O$_{104}$	I/O$_{107}$	I/O$_{110}$	NC	NC	I/O$_{115}$	I/O$_{118}$	I/O$_{120}$	W
Y	I/O$_{71}$	I/O$_{73}$	I/O$_{77}$	TMS	I/O$_{80}$	I/O$_{84}$	I/O$_{87}$	I/O$_{90}$	I/O$_{94}$	NC	NC	I/O$_{99}$	I/O$_{103}$	I/O$_{106}$	I/O$_{108}$	I/O$_{111}$	NC	NC	I/O$_{116}$	I/O$_{119}$	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Pin Configurations[19] (continued)

256-Ball Fine-Pitch BGA (BB256)
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	GND	I/O$_{26}$	I/O$_{24}$	I/O$_{20}$	V_{CC}	I/O$_{11}$	GND	GND	I/O$_{186}$	V_{CC}	I/O$_{177}$	I/O$_{172}$	I/O$_{167}$	GND	GND
B	GND	I/O$_{27}$	I/O$_{25}$	I/O$_{23}$	I/O$_{19}$	I/O$_{15}$	I/O$_{10}$	GND	GND	I/O$_{185}$	I/O$_{181}$	I/O$_{176}$	I/O$_{171}$	I/O$_{166}$	I/O$_{165}$	GND
C	I/O$_{29}$	I/O$_{28}$	NC	I/O$_{22}$	I/O$_{18}$	I/O$_{14}$	I/O$_{9}$	I/O$_{4}$	I/O$_{191}$	I/O$_{184}$	I/O$_{180}$	I/O$_{175}$	I/O$_{170}$	NC	I/O$_{163}$	I/O$_{164}$
D	I/O$_{32}$	I/O$_{31}$	I/O$_{30}$	NC	I/O$_{17}$	I/O$_{13}$	I/O$_{8}$	I/O$_{3}$	I/O$_{190}$	I/O$_{183}$	I/O$_{179}$	I/O$_{174}$	I/O$_{169}$	I/O$_{160}$	I/O$_{161}$	I/O$_{162}$
E	I/O$_{35}$	I/O$_{34}$	I/O$_{33}$	I/O$_{21}$	I/O$_{16}$	I/O$_{12}$	I/O$_{7}$	I/O$_{2}$	I/O$_{189}$	V_{CC}	I/O$_{178}$	I/O$_{173}$	I/O$_{168}$	I/O$_{157}$	I/O$_{158}$	I/O$_{159}$
F	V_{CC}	I/O$_{38}$	I/O$_{37}$	I/O$_{36}$	TCK	V_{CC}	I/O$_{6}$	I/O$_{1}$	I/O$_{188}$	I/O$_{182}$	V_{CC}	TDI	I/O$_{154}$	I/O$_{155}$	I/O$_{156}$	V_{CC}
G	I/O$_{43}$	I/O$_{42}$	I/O$_{41}$	I/O$_{40}$	V_{CC}	I/O$_{39}$	I/O$_{5}$	I/O$_{0}$	I/O$_{187}$	I/O$_{148}$	I/O$_{149}$	CLK$_{3}$ /I$_{4}$	I/O$_{150}$	I/O$_{151}$	I/O$_{152}$	I/O$_{153}$
H	GND	GND	I/O$_{47}$	I/O$_{46}$	CLK$_{0}$ /I$_{0}$	I/O$_{45}$	I/O$_{44}$	GND	GND	I/O$_{144}$	I/O$_{145}$	CLK$_{2}$ /I$_{3}$	I/O$_{146}$	I/O$_{147}$	GND	GND
J	GND	GND	I/O$_{51}$	I/O$_{50}$	NC	I/O$_{49}$	I/O$_{48}$	GND	GND	I/O$_{140}$	I/O$_{141}$	I$_{2}$	I/O$_{142}$	I/O$_{143}$	GND	GND
K	I/O$_{57}$	I/O$_{56}$	I/O$_{55}$	I/O$_{54}$	CLK$_{1}$ /I$_{1}$	I/O$_{53}$	I/O$_{52}$	I/O$_{91}$	I/O$_{96}$	I/O$_{101}$	I/O$_{135}$	V_{CC}	I/O$_{136}$	I/O$_{137}$	I/O$_{138}$	I/O$_{139}$
L	V_{CC}	I/O$_{60}$	I/O$_{59}$	I/O$_{58}$	TMS	V_{CC}	I/O$_{86}$	I/O$_{92}$	I/O$_{97}$	I/O$_{102}$	V_{CC}	TDO	I/O$_{132}$	I/O$_{133}$	I/O$_{134}$	V_{CC}
M	I/O$_{63}$	I/O$_{62}$	I/O$_{61}$	I/O$_{72}$	I/O$_{77}$	I/O$_{82}$	V_{CC}	I/O$_{93}$	I/O$_{98}$	I/O$_{103}$	I/O$_{108}$	I/O$_{112}$	I/O$_{117}$	I/O$_{129}$	I/O$_{130}$	I/O$_{131}$
N	I/O$_{66}$	I/O$_{65}$	I/O$_{64}$	I/O$_{73}$	I/O$_{78}$	I/O$_{83}$	I/O$_{87}$	I/O$_{94}$	I/O$_{99}$	I/O$_{104}$	I/O$_{109}$	I/O$_{113}$	NC	I/O$_{126}$	I/O$_{127}$	I/O$_{128}$
P	I/O$_{68}$	I/O$_{67}$	NC	I/O$_{74}$	I/O79	I/O$_{84}$	I/O$_{88}$	I/O$_{95}$	I/O$_{100}$	I/O$_{105}$	I/O$_{110}$	I/O$_{114}$	I/O$_{118}$	NC	I/O$_{124}$	I/O$_{125}$
R	GND	I/O$_{69}$	I/O$_{70}$	I/O$_{75}$	I/O$_{80}$	I/O$_{85}$	I/O$_{89}$	GND	GND	I/O$_{106}$	I/O$_{111}$	I/O$_{115}$	I/O$_{119}$	I/O$_{121}$	I/O$_{123}$	GND
T	GND	GND	I/O$_{71}$	I/O$_{76}$	I/O$_{81}$	V_{CC}	I/O$_{90}$	GND	GND	I/O$_{107}$	V_{CC}	I/O$_{116}$	I/O$_{120}$	I/O$_{122}$	GND	GND

Pin Configurations[19] (continued)

352-Lead BGA (BG352)
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	GND	GND	I/O$_{19}$	I/O$_{15}$	I/O$_{13}$	I/O$_{34}$	I/O$_{31}$	I/O$_{28}$	I/O$_{25}$	I/O$_{10}$	I/O$_{7}$	I/O$_{4}$	I/O$_{1}$	I/O$_{263}$	I/O$_{260}$	I/O$_{257}$	I/O$_{254}$	I/O$_{239}$	I/O$_{237}$	I/O$_{232}$	I/O$_{229}$	I/O$_{250}$	I/O$_{248}$	I/O$_{244}$	GND	GND
B	GND	NC	I/O$_{18}$	I/O$_{17}$	I/O$_{14}$	I/O$_{35}$	I/O$_{32}$	I/O$_{29}$	I/O$_{26}$	I/O$_{11}$	I/O$_{8}$	I/O$_{5}$	I/O$_{2}$	V_{CC}	I/O$_{261}$	I/O$_{258}$	I/O$_{255}$	I/O$_{252}$	I/O$_{234}$	I/O$_{231}$	I/O$_{228}$	I/O$_{249}$	I/O$_{246}$	I/O$_{245}$	I/O$_{240}$	GND
C	I/O$_{23}$	I/O$_{38}$	I/O$_{37}$	I/O$_{16}$	I/O$_{12}$	I/O$_{33}$	I/O$_{30}$	I/O$_{27}$	I/O$_{24}$	I/O$_{9}$	I/O$_{6}$	I/O$_{3}$	I/O$_{0}$	I/O$_{262}$	I/O$_{259}$	I/O$_{256}$	I/O$_{253}$	I/O$_{238}$	I/O$_{235}$	I/O$_{233}$	I/O$_{230}$	I/O$_{251}$	I/O$_{247}$	I/O$_{225}$	I/O$_{224}$	I/O$_{227}$
D	I/O$_{39}$	I/O$_{40}$	I/O$_{36}$	NC	NC	I/O$_{21}$	I/O$_{20}$	V_{CCO}	V_{CCO}	NC	GND	GND	V_{CCO}	V_{CCO}	GND	GND	NC	V_{CCO}	V_{CCO}	I/O$_{236}$	I/O$_{243}$	NC	NC	I/O$_{226}$	I/O$_{222}$	I/O$_{223}$
E	I/O$_{42}$	TCK	I/O$_{41}$	NC																			NC	TDI	I/O$_{221}$	I/O$_{220}$
F	I/O$_{45}$	I/O$_{44}$	I/O$_{43}$	I/O$_{22}$																			I/O$_{242}$	I/O$_{219}$	I/O$_{218}$	I/O$_{217}$
G	I/O$_{48}$	I/O$_{47}$	I/O$_{46}$	I/O$_{63}$																			I/O$_{241}$	I/O$_{216}$	I/O$_{215}$	I/O$_{214}$
H	I/O$_{49}$	I/O$_{50}$	I/O$_{51}$	V_{CCO}																			V_{CCO}	I/O$_{211}$	I/O$_{212}$	I/O$_{213}$
J	I/O$_{52}$	I/O$_{53}$	I/O$_{54}$	V_{CCO}																			V_{CCO}	I/O$_{208}$	I/O$_{209}$	I/O$_{210}$
K	I/O$_{55}$	I/O$_{56}$	I/O$_{57}$	NC																			NC	I/O$_{205}$	I/O$_{206}$	I/O$_{207}$
L	I0	I/O$_{59}$	I/O$_{58}$	GND							GND	GND	GND	GND	GND	GND							GND	I/O$_{204}$	I4	I/O$_{197}$
M	I/O$_{61}$	I/O$_{60}$	I1	GND							GND	GND	GND	GND	GND	GND							GND	I3	I/O$_{203}$	I/O$_{202}$
N	I/O$_{64}$	V_{CC}	I/O$_{62}$	V_{CCO}							GND	GND	GND	GND	GND	GND							V_{CCO}	I/O$_{201}$	I/O$_{200}$	I/O$_{199}$
P	I/O$_{65}$	I/O$_{66}$	I/O$_{67}$	V_{CCO}							GND	GND	GND	GND	GND	GND							V_{CCO}	I/O$_{196}$	V_{CC}	I/O$_{198}$
R	I/O$_{68}$	I/O$_{69}$	I/O$_{70}$	GND							GND	GND	GND	GND	GND	GND							GND	I/O$_{193}$	I/O$_{194}$	I/O$_{195}$
T	I/O$_{71}$	I/O$_{84}$	I/O$_{85}$	GND							GND	GND	GND	GND	GND	GND							GND	I/O$_{178}$	I/O$_{179}$	I/O$_{192}$
U	I/O$_{88}$	I/O$_{87}$	I/O$_{86}$	NC																			NC	I/O$_{177}$	I/O$_{176}$	I/O$_{175}$
V	I/O$_{91}$	I/O$_{90}$	I/O$_{89}$	V_{CCO}																			V_{CCO}	I/O$_{174}$	I/O$_{173}$	I/O$_{172}$
W	I/O$_{94}$	I/O$_{93}$	I/O$_{92}$	V_{CCO}																			V_{CCO}	I/O$_{171}$	I/O$_{170}$	I/O$_{169}$
Y	I/O$_{95}$	I/O$_{72}$	I/O$_{73}$	I/O$_{110}$																			I/O$_{153}$	I/O$_{190}$	I/O$_{191}$	I/O$_{168}$
AA	I/O$_{74}$	I/O$_{75}$	I/O$_{76}$	I/O$_{111}$																			I/O$_{152}$	I/O$_{187}$	I/O$_{188}$	I/O$_{189}$
AB	I/O$_{77}$	I/O$_{78}$	I/O$_{79}$	N/C																			NC	I/O$_{184}$	I/O$_{185}$	I/O$_{186}$
AC	I/O$_{81}$	I/O$_{80}$	I/O$_{108}$	N/C	NC	I/O$_{112}$	I/O$_{113}$	V_{CCO}	V_{CCO}	NC	GND	GND	V_{CCO}	V_{CCO}	GND	GND	NC	V_{CCO}	V_{CCO}	I/O$_{150}$	I/O$_{151}$	NC	NC	I/O$_{155}$	I/O$_{183}$	I/O$_{182}$
AD	I/O$_{109}$	I/O$_{82}$	I/O$_{83}$	I/O$_{117}$	I/O$_{97}$	I/O$_{100}$	I/O$_{102}$	I/O$_{105}$	I/O$_{120}$	I/O$_{123}$	I/O$_{126}$	I/O$_{129}$	I2	I/O$_{133}$	I/O$_{136}$	I/O$_{139}$	I/O$_{142}$	I/O$_{157}$	I/O$_{159}$	I/O$_{161}$	I/O$_{163}$	I/O$_{166}$	I/O$_{146}$	I/O$_{180}$	I/O$_{181}$	I/O$_{154}$
AE	GND	NC	I/O$_{115}$	I/O$_{116}$	I/O$_{119}$	I/O$_{98}$	I/O$_{101}$	I/O$_{103}$	I/O$_{106}$	I/O$_{121}$	I/O$_{124}$	I/O$_{127}$	V_{CC}	I/O$_{130}$	I/O$_{134}$	I/O$_{137}$	I/O$_{140}$	I/O$_{143}$	I/O$_{160}$	I/O$_{162}$	I/O$_{165}$	I/O$_{144}$	I/O$_{147}$	I/O$_{148}$	NC	GND
AF	GND	GND	I/O$_{114}$	I/O$_{118}$	I/O$_{96}$	I/O$_{99}$	TMS	I/O$_{104}$	I/O$_{107}$	I/O$_{122}$	I/O$_{125}$	I/O$_{128}$	I/O$_{131}$	I/O$_{132}$	I/O$_{135}$	I/O$_{138}$	I/O$_{141}$	I/O$_{156}$	I/O$_{158}$	TDO	I/O$_{164}$	I/O$_{167}$	I/O$_{145}$	I/O$_{149}$	GND	GND

Pin Configurations[19] (continued)

400-Ball Fine-Pitch BGA (BB400)

Top View

A	GND	GND	NC	I/O_{17}	I/O_{16}	I/O_{14}	I/O_{29}	V_{CC}	I/O_{11}	GND	GND	I/O_{257}	V_{CC}	I/O_{239}	I/O_{233}	I/O_{232}	I/O_{230}	NC	GND	GND
B	GND	GND	GND	NC	I/O_{15}	I/O_{13}	I/O_{28}	V_{CC}	I/O_{10}	GND	GND	I/O_{256}	V_{CC}	I/O_{238}	I/O_{231}	I/O_{229}	NC	GND	GND	GND
C	NC	GND	GND	GND	I/O_{20}	I/O_{12}	I/O_{27}	V_{CC}	I/O_{9}	GND	GND	I/O_{255}	V_{CC}	I/O_{237}	I/O_{228}	I/O_{245}	GND	GND	GND	NC
D	I/O_{44}	NC	GND	I/O_{21}	I/O_{19}	I/O_{18}	I/O_{26}	I/O_{25}	I/O_{8}	GND	GND	I/O_{254}	I/O_{235}	I/O_{236}	I/O_{251}	I/O_{244}	I/O_{243}	GND	NC	I/O_{227}
E	I/O_{46}	I/O_{43}	I/O_{23}	I/O_{22}	NC	I/O_{35}	I/O_{34}	I/O_{24}	I/O_{7}	I/O_{4}	I/O_{263}	I/O_{253}	I/O_{234}	I/O_{250}	I/O_{248}	NC	I/O_{241}	I/O_{242}	I/O_{225}	I/O_{226}
F	I/O_{47}	I/O_{45}	I/O_{42}	I/O_{41}	I/O_{40}	NC	I/O_{33}	I/O_{32}	I/O_{6}	I/O_{3}	I/O_{262}	I/O_{252}	I/O_{249}	I/O_{247}	I/O_{220}	I/O_{221}	I/O_{240}	I/O_{222}	I/O_{223}	I/O_{224}
G	I/O_{53}	I/O_{52}	I/O_{51}	I/O_{50}	I/O_{39}	I/O_{38}	I/O_{37}	I/O_{31}	I/O_{5}	I/O_{2}	I/O_{261}	V_{CC}	I/O_{246}	I/O_{217}	I/O_{218}	I/O_{219}	I/O_{212}	I/O_{213}	I/O_{214}	I/O_{215}
H	V_{CC}	V_{CC}	V_{CC}	I/O_{49}	I/O_{48}	I/O_{36}	TCK	V_{CC}	I/O_{30}	I/O_{1}	I/O_{259}	I/O_{260}	V_{CC}	TDI	I/O_{216}	I/O_{210}	I/O_{211}	V_{CC}	V_{CC}	V_{CC}
J	I/O_{59}	I/O_{58}	I/O_{57}	I/O_{56}	I/O_{55}	I/O_{54}	V_{CC}	I/O_{62}	I/O_{60}	I/O_{0}	I/O_{258}	I/O_{202}	I/O_{203}	CLK_{3} $/I_{4}$	I/O_{204}	I/O_{205}	I/O_{206}	I/O_{207}	I/O_{208}	I/O_{209}
K	GND	GND	GND	GND	I/O_{65}	I/O_{64}	CLK_{0} $/I_{0}$	I/O_{63}	I/O_{61}	GND	GND	I/O_{198}	I/O_{199}	CLK_{2} $/I_{3}$	I/O_{200}	I/O_{201}	GND	GND	GND	GND
L	GND	GND	GND	GND	I/O_{69}	I/O_{68}	NC	I/O_{67}	I/O_{66}	GND	GND	I/O_{193}	I/O_{195}	I_{2}	I/O_{196}	I/O_{197}	GND	GND	GND	GND
M	I/O_{89}	I/O_{88}	I/O_{87}	I/O_{86}	I/O_{85}	I/O_{84}	CLK_{1} $/I_{1}$	I/O_{71}	I/O_{70}	I/O_{126}	I/O_{132}	I/O_{192}	I/O_{194}	V_{CC}	I/O_{174}	I/O_{175}	I/O_{176}	I/O_{177}	I/O_{178}	I/O_{179}
N	V_{CC}	V_{CC}	V_{CC}	I/O_{91}	I/O_{90}	I/O_{72}	TMS	V_{CC}	I/O_{128}	I/O_{127}	I/O_{133}	I/O_{162}	V_{CC}	TDO	I/O_{180}	I/O_{168}	I/O_{169}	V_{CC}	V_{CC}	V_{CC}
P	I/O_{95}	I/O_{94}	I/O_{93}	I/O_{92}	I/O_{75}	I/O_{74}	I/O_{73}	I/O_{114}	V_{CC}	I/O_{129}	I/O_{134}	I/O_{137}	I/O_{163}	I/O_{181}	I/O_{182}	I/O_{183}	I/O_{170}	I/O_{171}	I/O_{172}	I/O_{173}
R	I/O_{80}	I/O_{79}	I/O_{78}	I/O_{108}	I/O_{77}	I/O_{76}	I/O_{115}	I/O_{117}	I/O_{120}	I/O_{130}	I/O_{135}	I/O_{138}	I/O_{164}	I/O_{165}	NC	I/O_{184}	I/O_{185}	I/O_{186}	I/O_{189}	I/O_{191}
T	I/O_{82}	I/O_{81}	I/O_{110}	I/O_{109}	NC	I/O_{116}	I/O_{118}	I/O_{102}	I/O_{121}	I/O_{131}	I/O_{136}	I/O_{139}	I/O_{156}	I/O_{166}	I/O_{167}	NC	I/O_{154}	I/O_{155}	I/O_{187}	I/O_{190}
U	I/O_{83}	NC	GND	I/O_{111}	I/O_{112}	I/O_{119}	I/O_{104}	I/O_{103}	I/O_{122}	GND	GND	I/O_{140}	I/O_{157}	I/O_{158}	I/O_{150}	I/O_{151}	I/O_{153}	GND	NC	I/O_{188}
V	NC	GND	GND	GND	I/O_{113}	I/O_{96}	I/O_{105}	V_{CC}	I/O_{123}	GND	GND	I/O_{141}	V_{CC}	I/O_{159}	I/O144	I/O_{152}	GND	GND	GND	NC
W	GND	GND	GND	NC	I/O_{97}	I/O_{99}	I/O_{106}	V_{CC}	I/O_{124}	GND	GND	I/O_{142}	V_{CC}	I/O_{160}	I/O_{145}	I/O_{147}	NC	GND	GND	GND
Y	GND	GND	NC	I/O_{98}	I/O_{100}	I/O_{101}	I/O_{107}	V_{CC}	I/O_{125}	GND	GND	I/O_{143}	V_{CC}	I/O_{161}	I/O_{146}	I/O_{148}	I/O_{149}	NC	GND	GND

Ordering Information

CY 37 512 V P400 - 83 BB C

Cypress Semiconductor ID

Family Type
37 = Ultra37000 Family

Macrocell Density
32 = 32 Macrocells
64 = 64 Macrocells
128 = 128 Macrocells
192 = 192 Macrocells
256 = 256 Macrocells
384 = 384 Macrocells
512 = 512 Macrocells

Operating Reference Voltage
V = 3.3V Supply Voltage
(5.0V if not specified)

Pin Count
P44 = 44 Leads
P48 = 48 Leads
P84 = 84 Leads
P100 = 100 Leads
P160 = 160 Leads
P208 = 208 Leads
P256 = 256 Leads
P352 = 352 Leads
P400 = 400 Leads

Operating Conditions
Commercial 0°C to +70°C
Industrial -40°C to +85°C
Military -55°C to +125°C

Package Type
A = Thin Quad Flat Pack (TQFP)
U = Ceramic Quad Flat Pack (CQFP)
N = Plastic Quad Flat Pack (PQFP)
NT = Thermally Enhanced Plastic Quad Flat Pack (EQFP)
J = Plastic Leaded Chip Carrier (PLCC)
Y = Ceramic Leaded Chip Carrier (CLCC)
BG = Ball Grid Array (BGA)
BA = Fine-Pitch Ball Grid Array (FBGA) 0.8mm Lead Pitch
BB = Fine-Pitch Ball Grid Array (FBGA) 1.0mm Lead Pitch

Speed
200 = 200 MHz
167 = 167 MHz
154 = 154 MHz
143 = 143 MHz
125 = 125 MHz
100 = 100 MHz
83 = 83 MHz
66 = 66 MHz

5.0V Ordering Information

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
32	200	CY37032P44-200AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-200JC	J67	44-Lead Plastic Leaded Chip Carrier	
	154	CY37032P44-154AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-154JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-154AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032P44-154JI	J67	44-Lead Plastic Leaded Chip Carrier	
	125	CY37032P44-125AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-125JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-125AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032P44-125JI	J67	44-Lead Plastic Leaded Chip Carrier	

5.0V Ordering Information (continued)

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
64	200	CY37064P44-200AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-200JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-200JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-200AC	A100	100-Lead Thin Quad Flat Pack	
	154	CY37064P44-154AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-154JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-154JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P44-154AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-154JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-154JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AI	A100	100-Lead Thin Quad Flat Pack	
		5962-9951902QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military
	125	CY37064P44-125AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-125JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P44-125AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-125JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-125JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AI	A100	100-Lead Thin Quad Flat Pack	
		5962-9951901QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military
128	167	CY37128P84-167JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P100-167AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P160-167AC	A160	160-Lead Thin Quad Flat Pack	
	125	CY37128P84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P160-125AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128P84-125JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
		CY37128P100-125AI	A100	100-Lead Thin Quad Flat Pack	
		CY37128P160-125AI	A160	160-Lead Thin Quad Flat Pack	
		5962-9952102QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
	100	CY37128P84-100JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P100-100AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P160-100AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128P84-100JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
		CY37128P100-100AI	A100	100-Lead Thin Quad Flat Pack	
		CY37128P160-100AI	A160	160-Lead Thin Quad Flat Pack	
		5962-9952101QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military

5.0V Ordering Information (continued)

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
192	154	CY37192P160-154AC	A160	160-Lead Thin Quad Flat Pack	Commercial
	125	CY37192P160-125AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192P160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
	83	CY37192P160-83AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192P160-83AI	A160	160-Lead Thin Quad Flat Pack	Industrial
256	154	CY37256P160-154AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P208-154NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-154BGC	BG256	256-Lead Ball Grid Array	
	125	CY37256P160-125AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P208-125NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-125BGC	BG256	256-Lead Ball Grid Array	
		CY37256P160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256P208-125NI	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-125BGI	BG256	256-Lead Ball Grid Array	
		5962-9952302QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
	83	CY37256P160-83AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P208-83NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-83BGC	BG256	256-Lead Ball Grid Array	
		CY37256P160-83AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256P208-83NI	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-83BGI	BG256	256-Lead Ball Grid Array	
		5962-9952301QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	125	CY37384P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384P256-125BGC	BG256	256-Lead Ball Grid Array	
	83	CY37384P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384P256-83BGC	BG256	256-Lead Ball Grid Array	
		CY37384P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384P256-83BGI	BG256	256-Lead Ball Grid Array	

5.0V Ordering Information (continued)

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
512	125	CY37512P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-125BGC	BG256	256-Lead Ball Grid Array	
		CY37512P352-125BGC	BG352	352-Lead Ball Grid Array	
	100	CY37512P208-100NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-100BGC	BG256	256-Lead Ball Grid Array	
		CY37512P352-100BGC	BG352	352-Lead Ball Grid Array	
		CY37512P208-100NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-100BGI	BG256	256-Lead Ball Grid Array	
		CY37512P352-100BGI	BG352	352-Lead Ball Grid Array	
		5962-9952502QZC	U208	208-Lead Ceramic Quad Flat Pack	Military
	83	CY37512P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-83BGC	BG256	256-Lead Ball Grid Array	
		CY37512P352-83BGC	BG352	352-Lead Ball Grid Array	
		CY37512P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-83BGI	BG256	256-Lead Ball Grid Array	
		CY37512P352-83BGI	BG352	352-Lead Ball Grid Array	
		5962-9952501QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

3.3V Ordering Information

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
32	143	CY37032VP44-143AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-143JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032VP48-143BAC	BA50	48-Lead Fine Pitch Ball Grid Array	
	100	CY37032VP44-100AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-100JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032VP48-100BAC	BA50	48-Lead Fine Pitch Ball Grid Array	
		CY37032VP44-100AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032VP44-100JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032VP48-100BAI	BA50	48-Lead Fine Pitch Ball Grid Array	

3.3V Ordering Information (continued)

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
64	143	CY37064VP44-143AC	A44	44-Lead Thin Quad Flatpack	Commercial
		CY37064VP44-143JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064VP48-143BAC	BA50	48-Lead Fine-Pitch Ball Grid Array	
		CY37064VP84-143JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064VP100-143AC	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-143BBC	BB100	100-Lead Fine-Pitch Ball Grid Array	
	100	CY37064VP44-100AC	A44	44-Lead Thin Quad Flatpack	Commercial
		CY37064VP44-100JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064VP48-100BAC	BA50	48-Lead Fine-Pitch Ball Grid Array	
		CY37064VP84-100JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064VP100-100AC	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-100BBC	BB100	100-Lead Fine-Pitch Ball Grid Array	
		CY37064VP44-100AI	A44	44-Lead Thin Quad Flatpack	Industrial
		CY37064VP44-100JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064VP48-100BAI	BA50	48-Lead Fine-Pitch Ball Grid Array	
		CY37064VP84-100JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064VP100-100BBI	BB100	100-Lead Fine-Pitch Ball Grid Array	
		CY37064VP100-100AI	A100	100-Lead Thin Quad Flatpack	
		5962-9952001QYA	Y67	44-Lead Ceramic Leaded Chip Carrier	Military
128	125	CY37128VP84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128VP100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128VP100-125BBC	BB100	100-Lead Fine-Pitch Ball Grid Array	
		CY37128VP160-125AC	A160	160-Lead Thin Quad Flat Pack	
	83	CY37128VP84-83JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128VP100-83AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128VP100-83BBC	BB100	100-Lead Fine-Pitch Ball Grid Array	
		CY37128VP160-83AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128VP84-83JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
		CY37128VP100-83AI	A100	100-Lead Thin Quad Flat Pack	
		CY37128VP100-83BBI	BB100	100-Lead Fine-Pitch Ball Grid Array	
		CY37128VP160-83AI	A160	160-Lead Thin Quad Flat Pack	
		5962-9952201QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
192	100	CY37192VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
	66	CY37192VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial

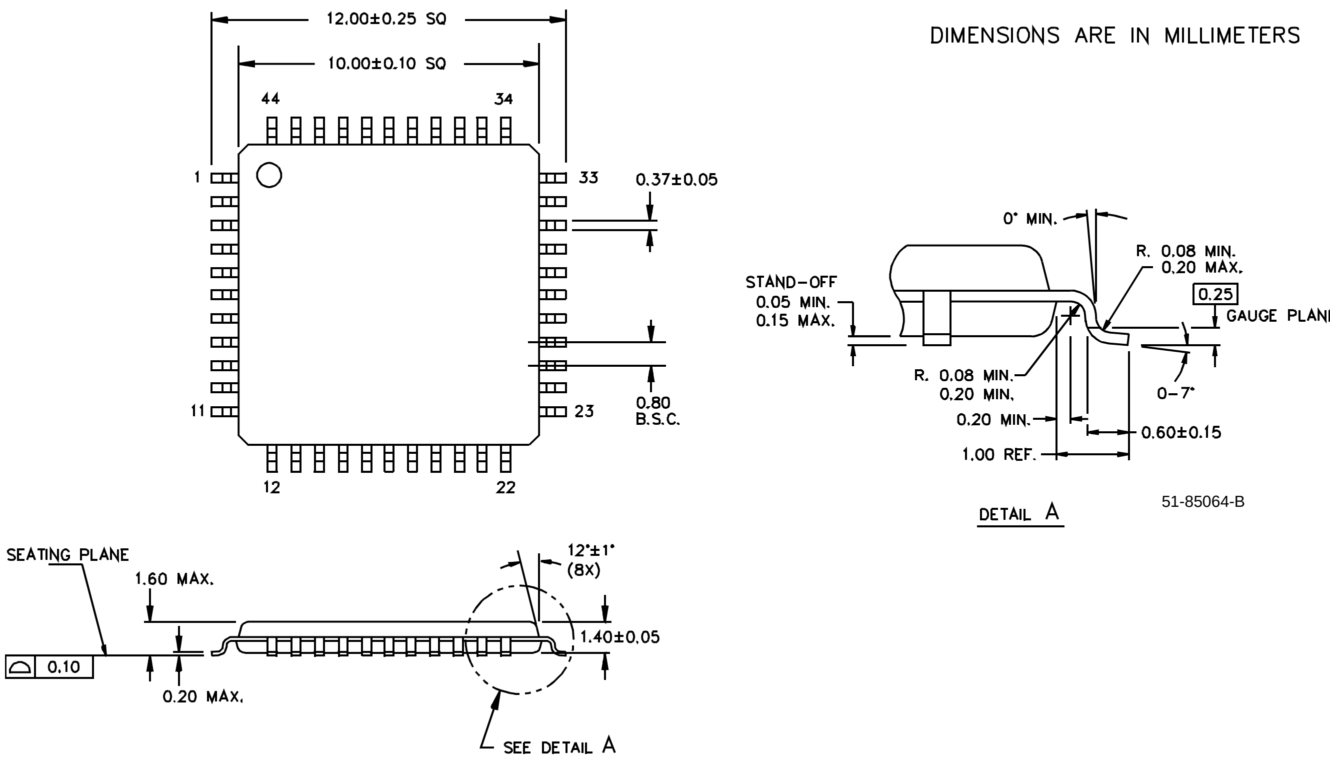
3.3V Ordering Information (continued)

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	100	CY37256VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP208-100NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-100BGC	BG256	256-Lead Ball Grid Array	
		CY37256VP256-100BBC	BB256	256-Lead Fine-Pitch Ball Grid Array	
	66	CY37256VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-66BGC	BG256	256-Lead Ball Grid Array	
		CY37256VP256-66BBC	BB256	256-Lead Fine-Pitch Ball Grid Array	
		CY37256VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP256-66BGI	BG256	256-Lead Ball Grid Array	
		CY37256VP256-66BBI	BB256	256-Lead Fine-Pitch Ball Grid Array	
		5962-9952401QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	83	CY37384VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-83BGC	BG256	256-Lead Ball Grid Array	
	66	CY37384VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-66BGC	BG256	256-Lead Ball Grid Array	
		CY37384VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384VP256-66BGI	BG256	256-Lead Ball Grid Array	
512	83	CY37512VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-83BGC	BG256	256-Lead Ball Grid Array	
		CY37512VP352-83BGC	BG352	352-Lead Ball Grid Array	
		CY37512VP400-83BBC	BB400	400-Lead Fine-Pitch Ball Grid Array	
	66	CY37512VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-66BGC	BG256	256-Lead Ball Grid Array	
		CY37512VP352-66BGC	BG352	352-Lead Ball Grid Array	
		CY37512VP400-66BBC	BB400	400-Lead Fine-Pitch Ball Grid Array	
		CY37512VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512VP256-66BGI	BG256	256-Lead Ball Grid Array	
		CY37512VP352-66BGI	BG352	352-Lead Ball Grid Array	
		CY37512VP400-66BBI	BB400	400-Lead Fine-Pitch Ball Grid Array	
		5962-9952601QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

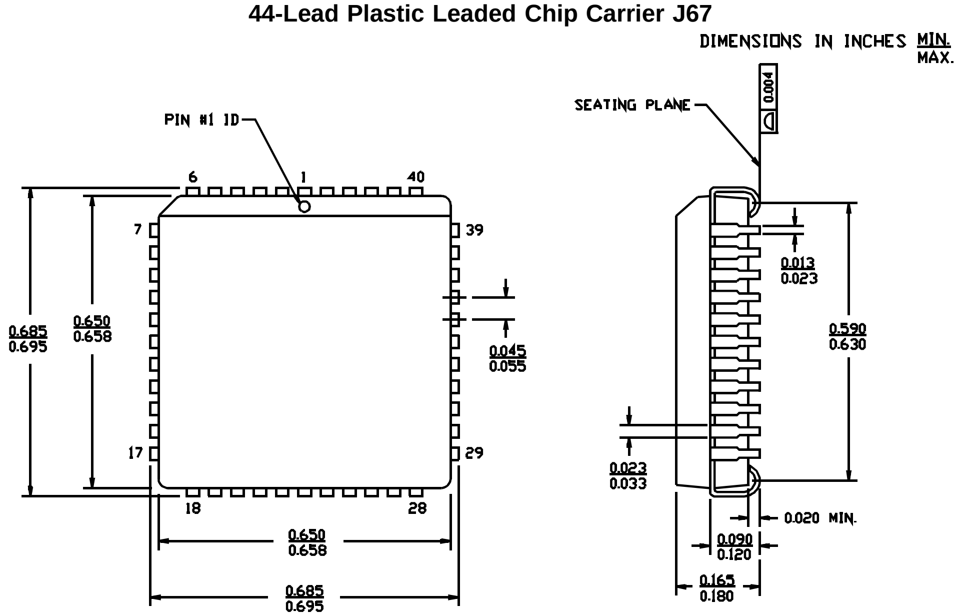
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Package Diagrams

44-Lead Thin Plastic Quad Flat Pack A44



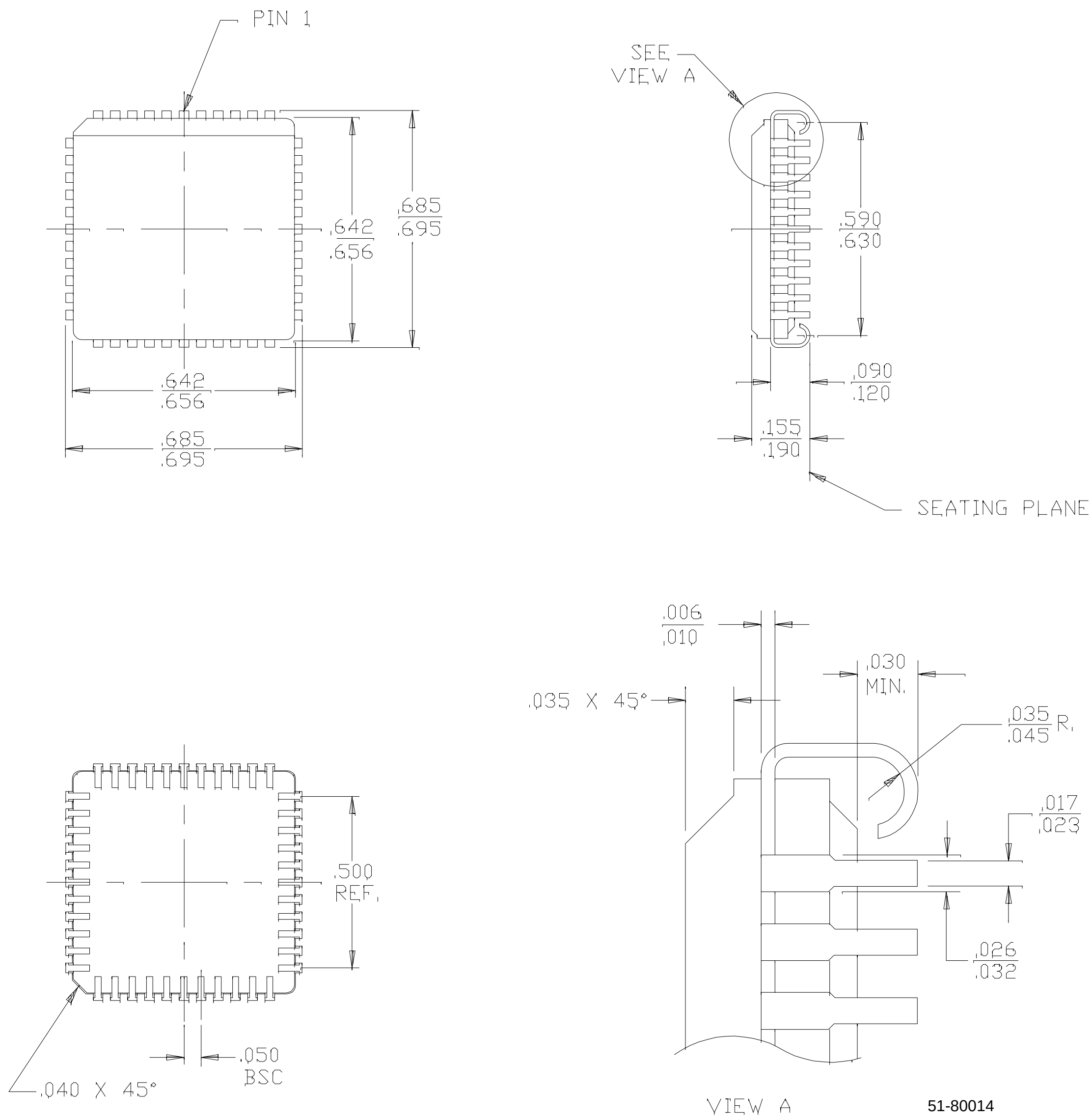
44-Lead Plastic Leaded Chip Carrier J67



51-85003-A

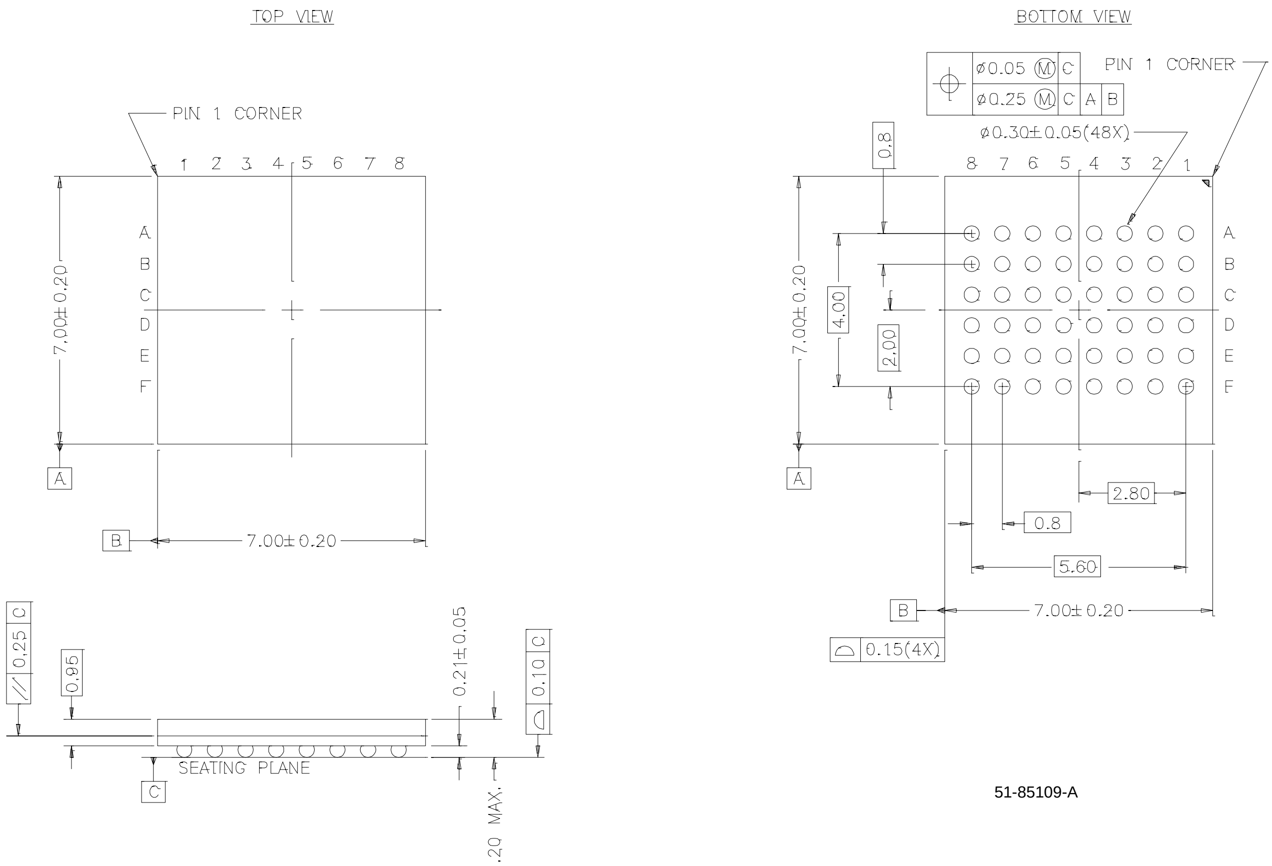
Package Diagrams (continued)

44-Pin Ceramic Leaded Chip Carrier Y67



Package Diagrams (continued)

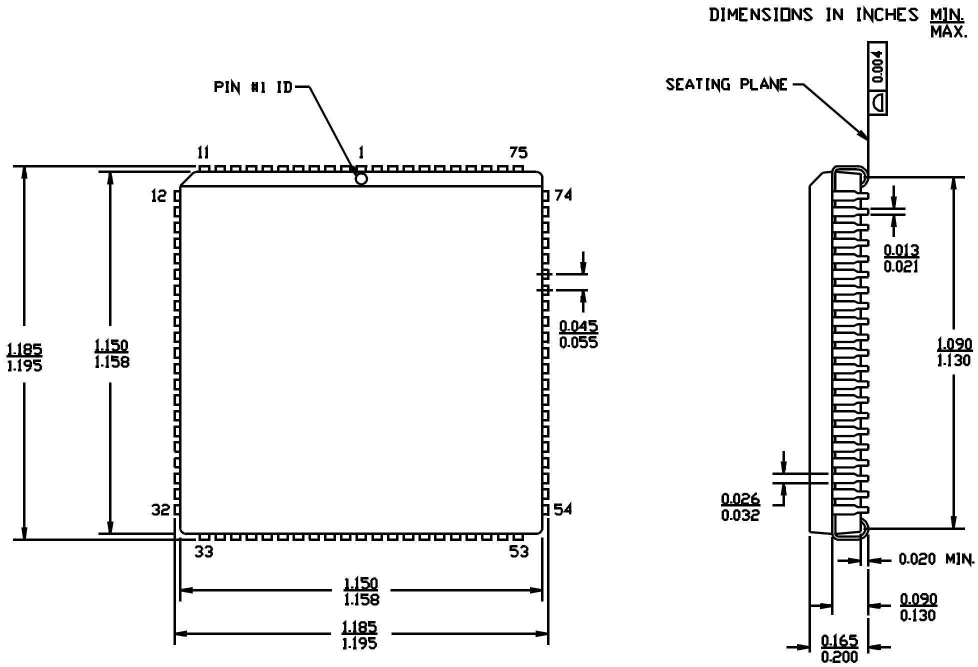
48-Ball (7.0 mm x 7.0 mm x 1.1 mm, 0.80 pitch) Thin BGA BA50



51-85109-A

Package Diagrams (continued)

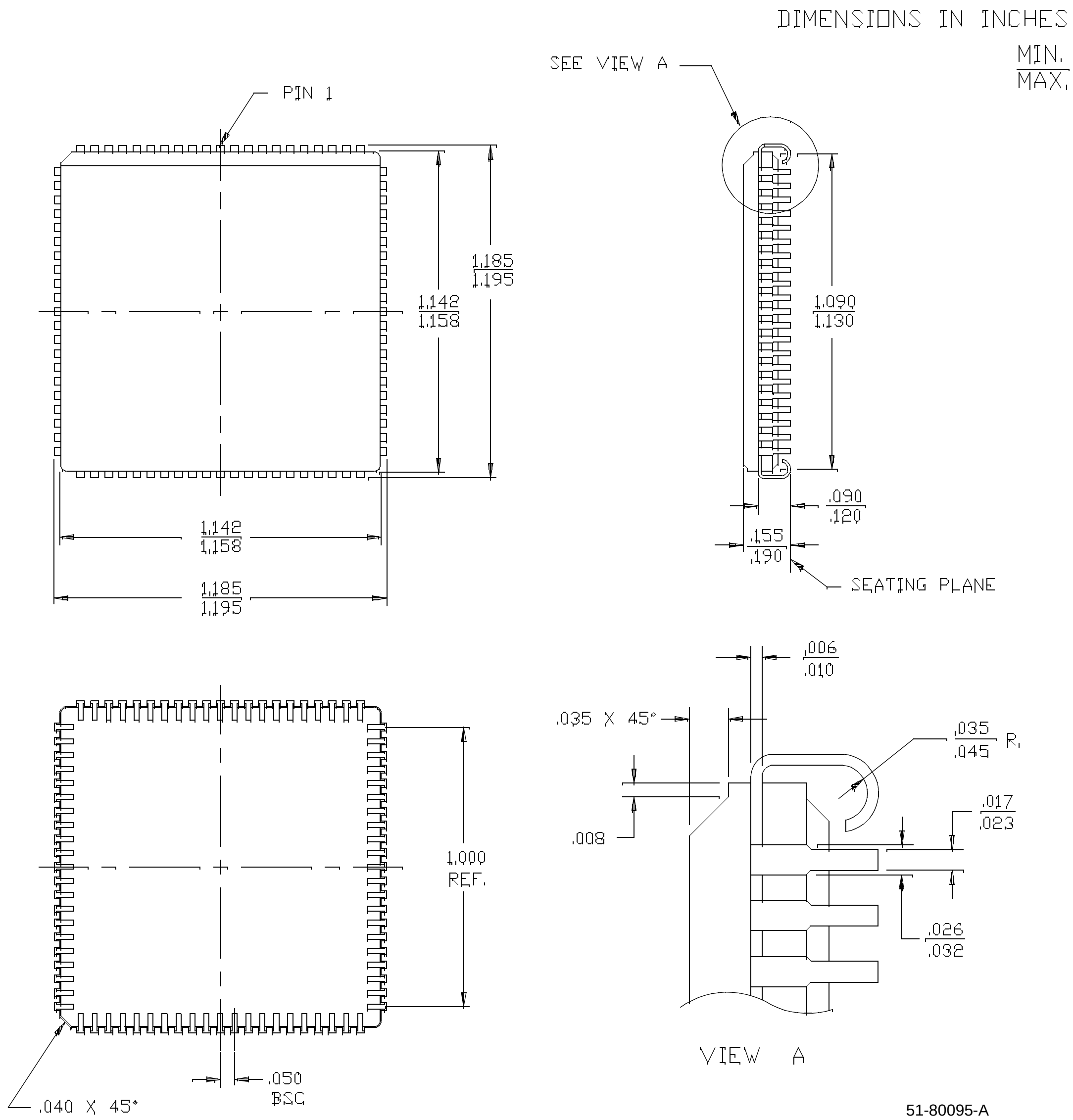
84-Lead Plastic Leaded Chip Carrier J83



51-85006-A

Package Diagrams (continued)

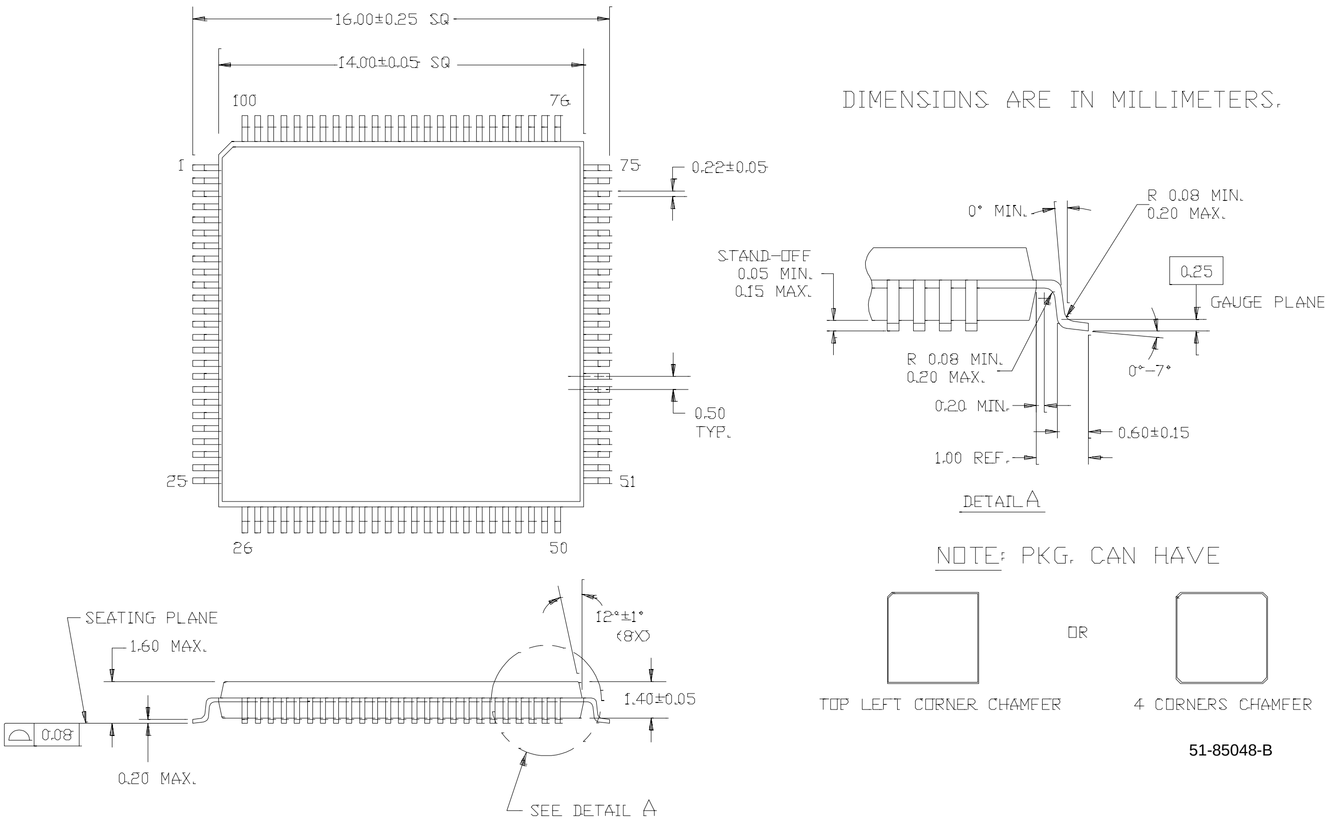
84-Pin Ceramic Leaded Chip Carrier Y84



51-80095-A

Package Diagrams (continued)

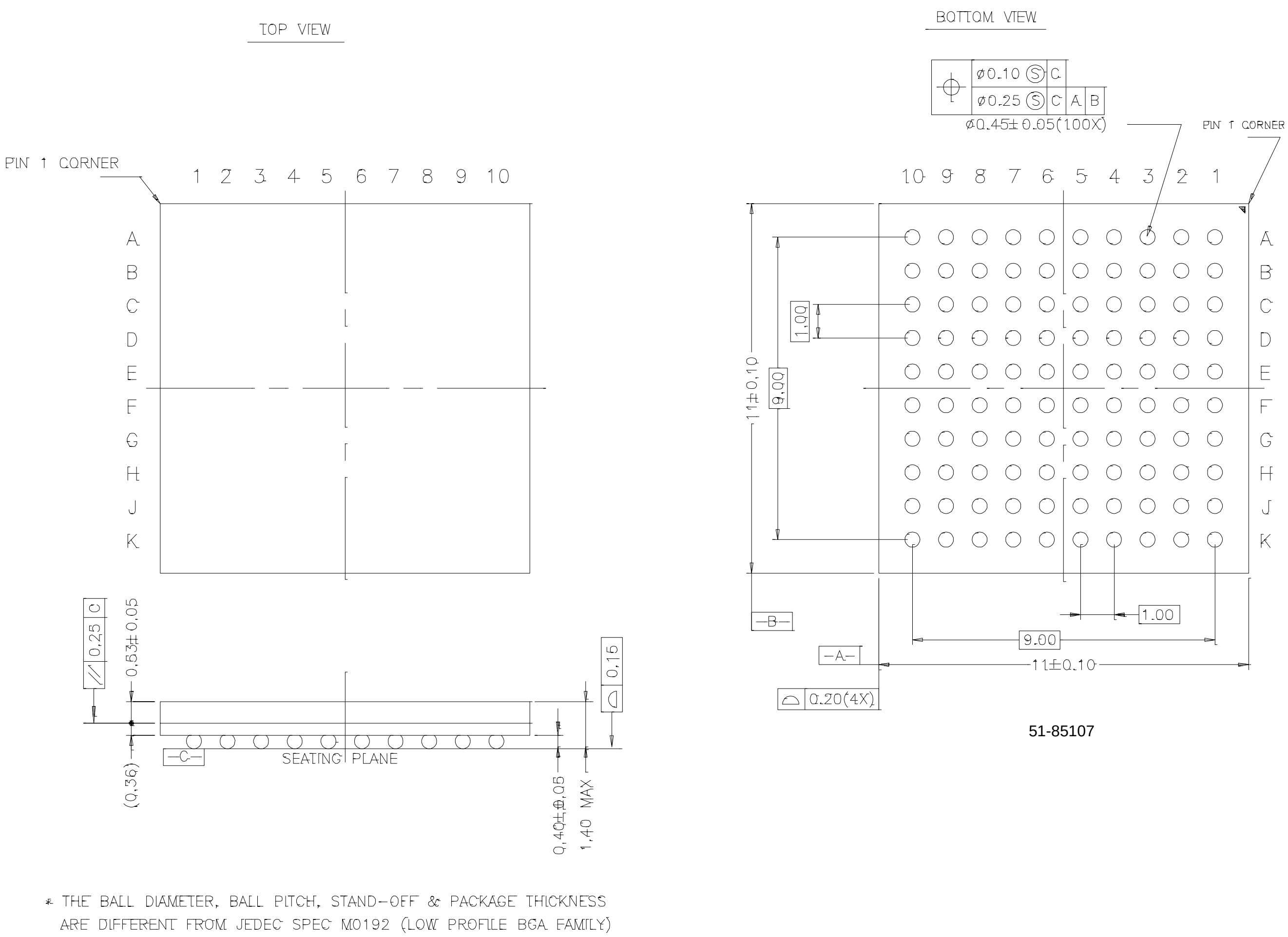
100-Pin Thin Plastic Quad Flat Pack (TQFP) A100



51-85048-B

Package Diagrams (continued)

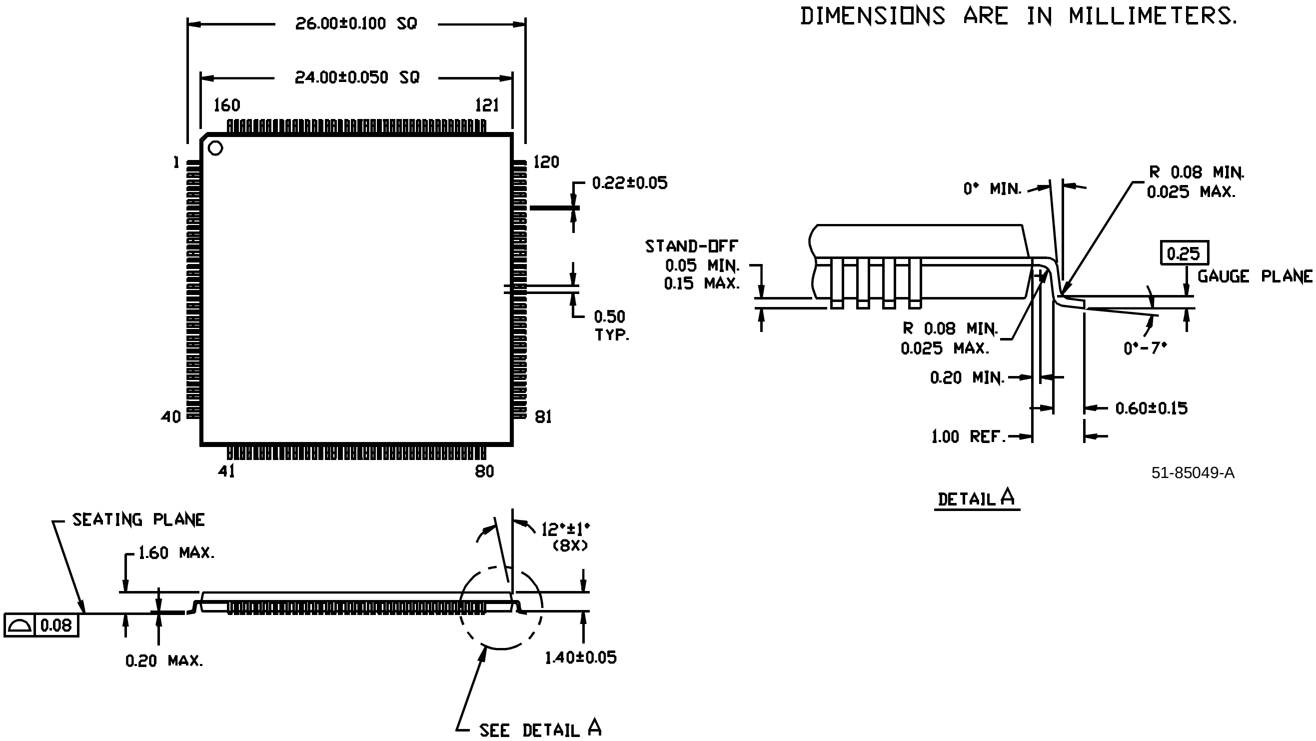
100-Ball Thin Ball Grid Array (11 x 11 x 1.4 mm) BB100



51-85107

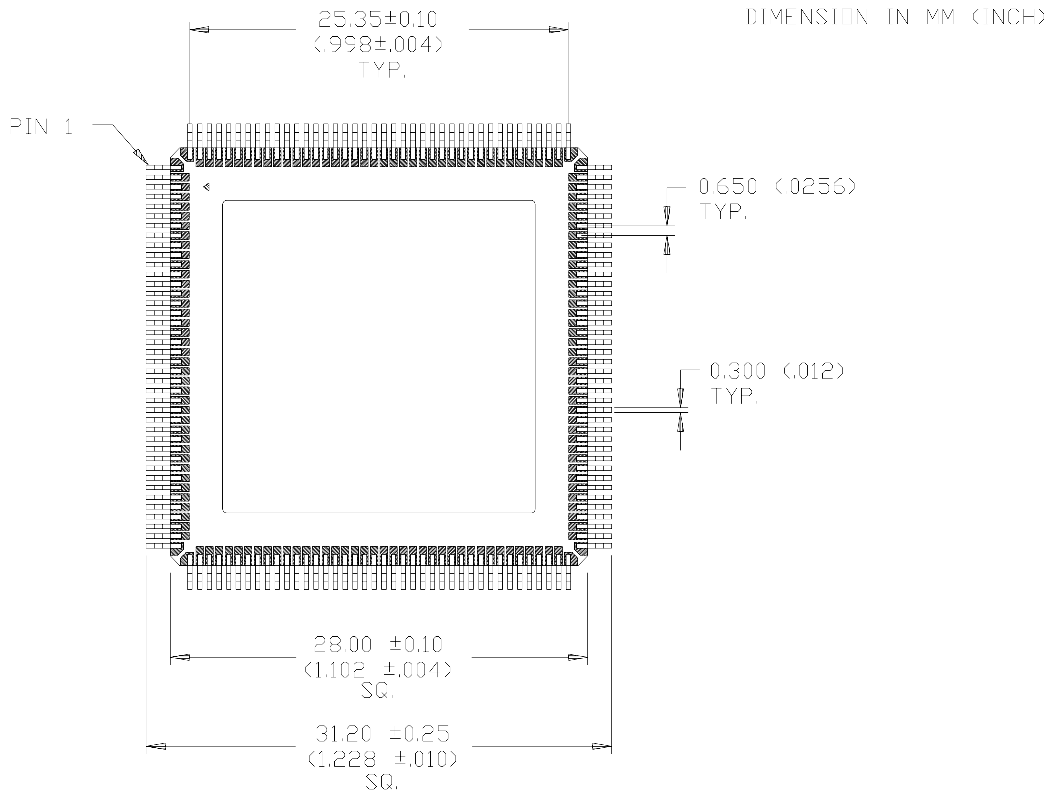
Package Diagrams (continued)

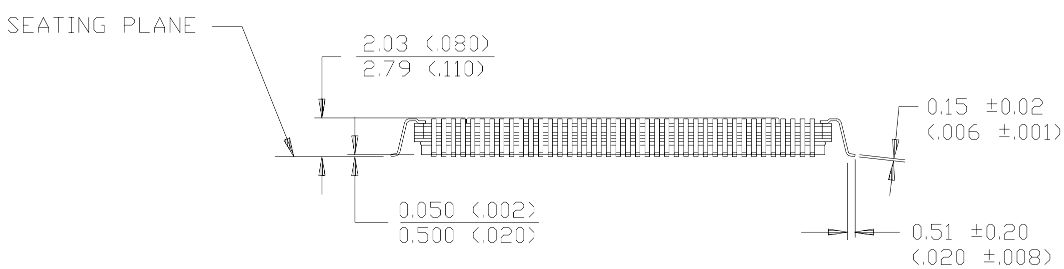
160-Pin Thin Plastic Quad Flat Pack (TQFP) A160



Package Diagrams (continued)

160-Lead Ceramic Quad Flatpack (Cavity Up) U162

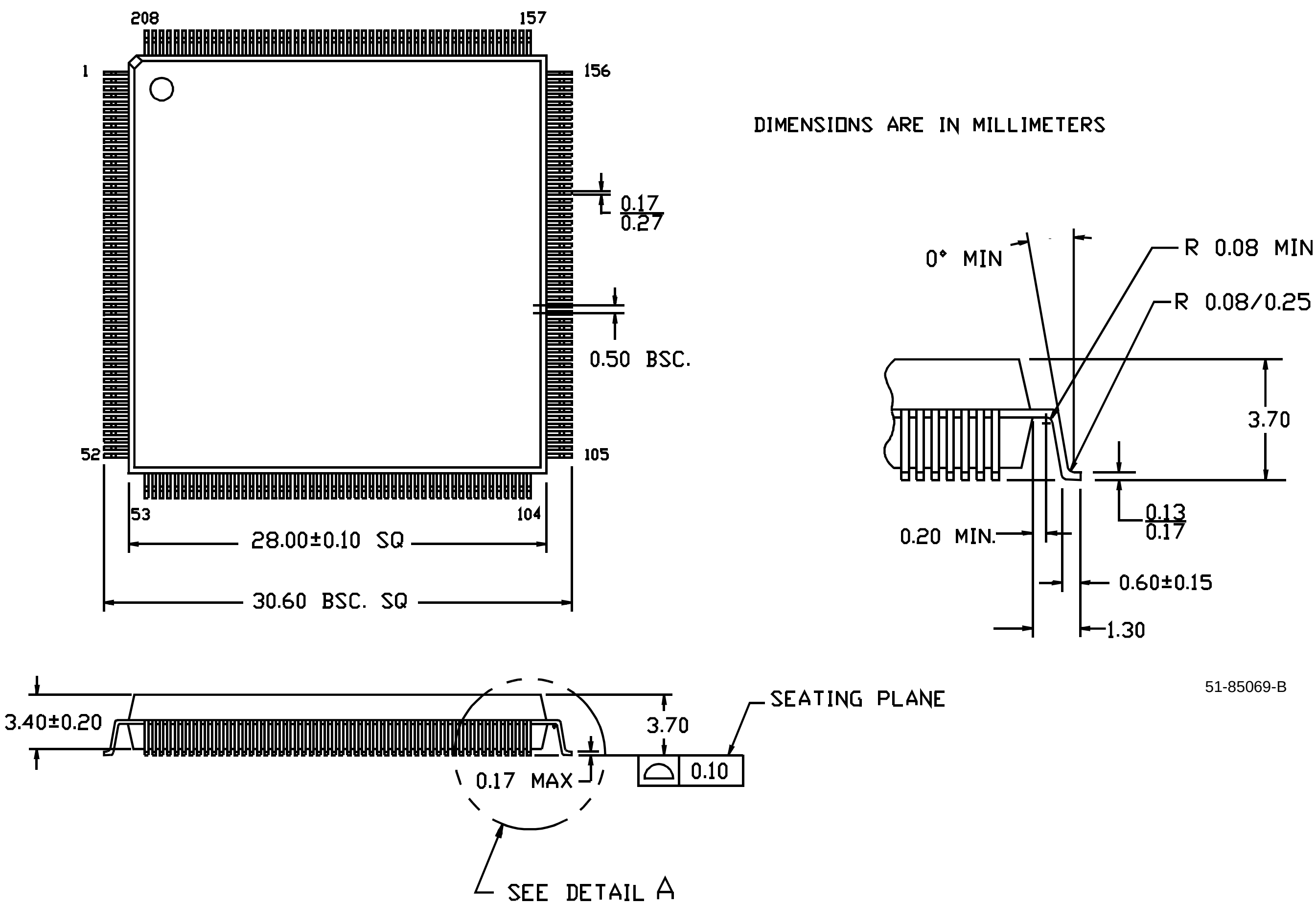




51-80106

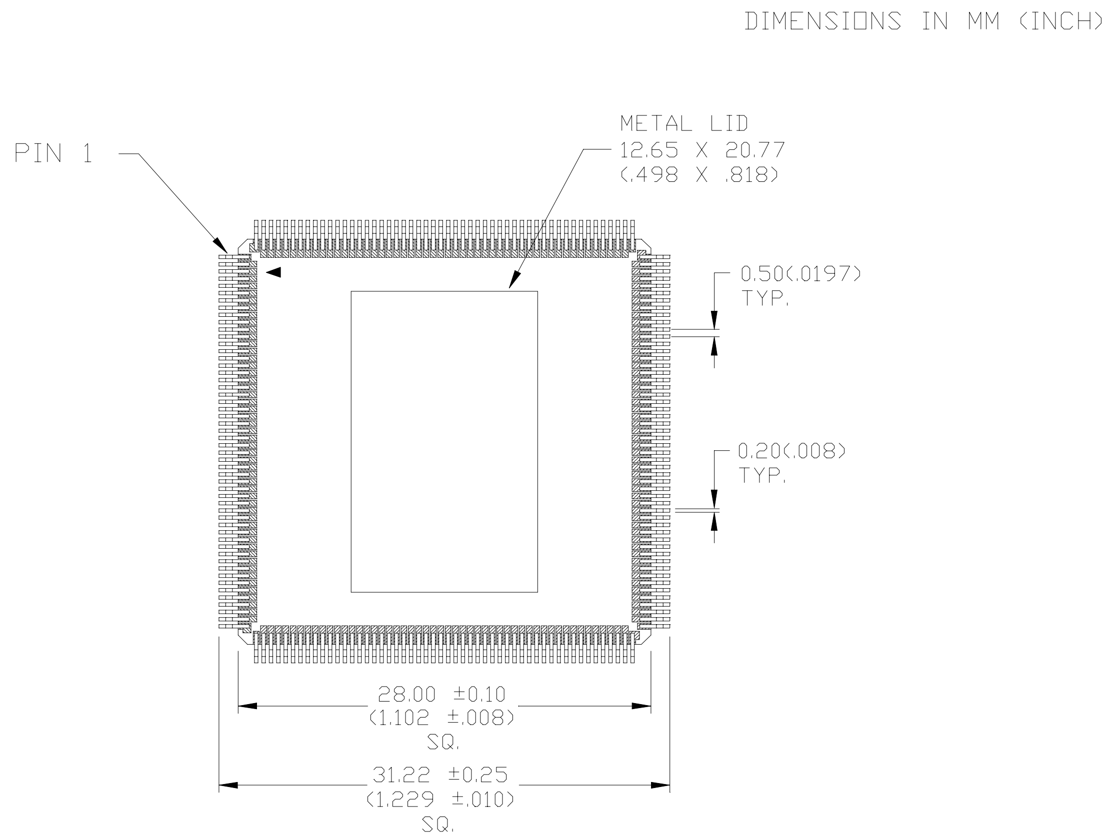
Package Diagrams (continued)

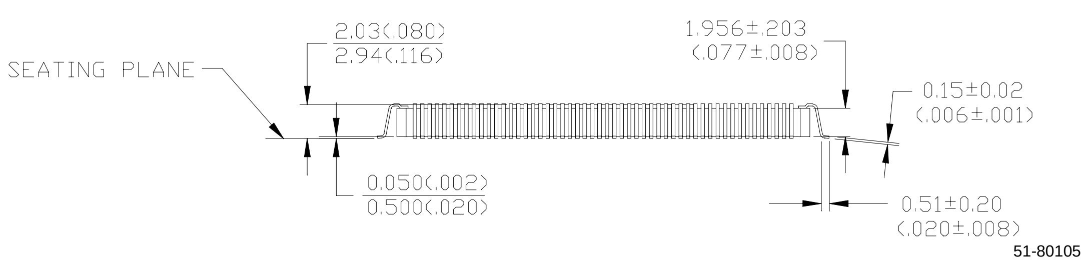
208-Lead Plastic Quad Flatpack N208



Package Diagrams (continued)

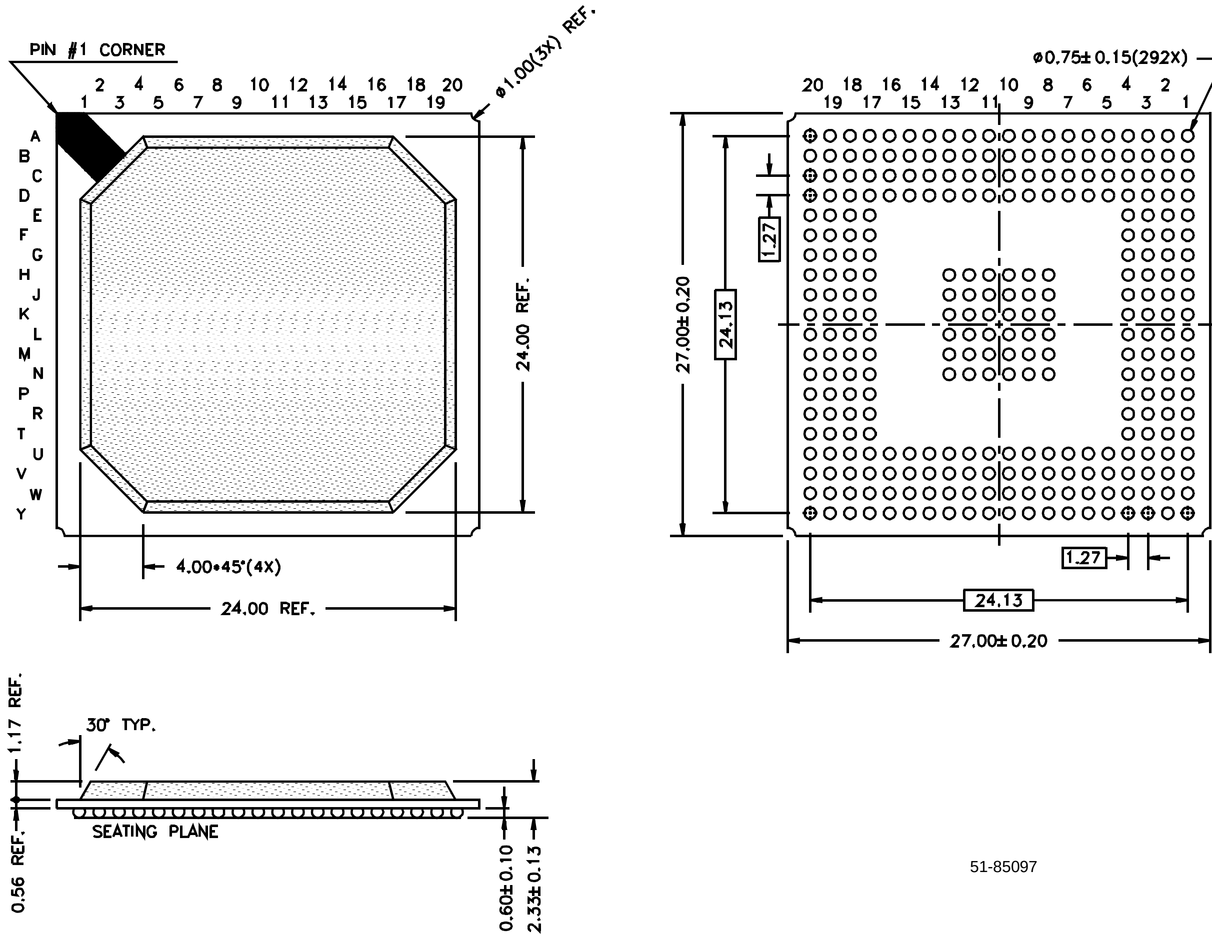
208-Lead Ceramic Quad Flatpack (Cavity Up) U208





Package Diagrams (continued)

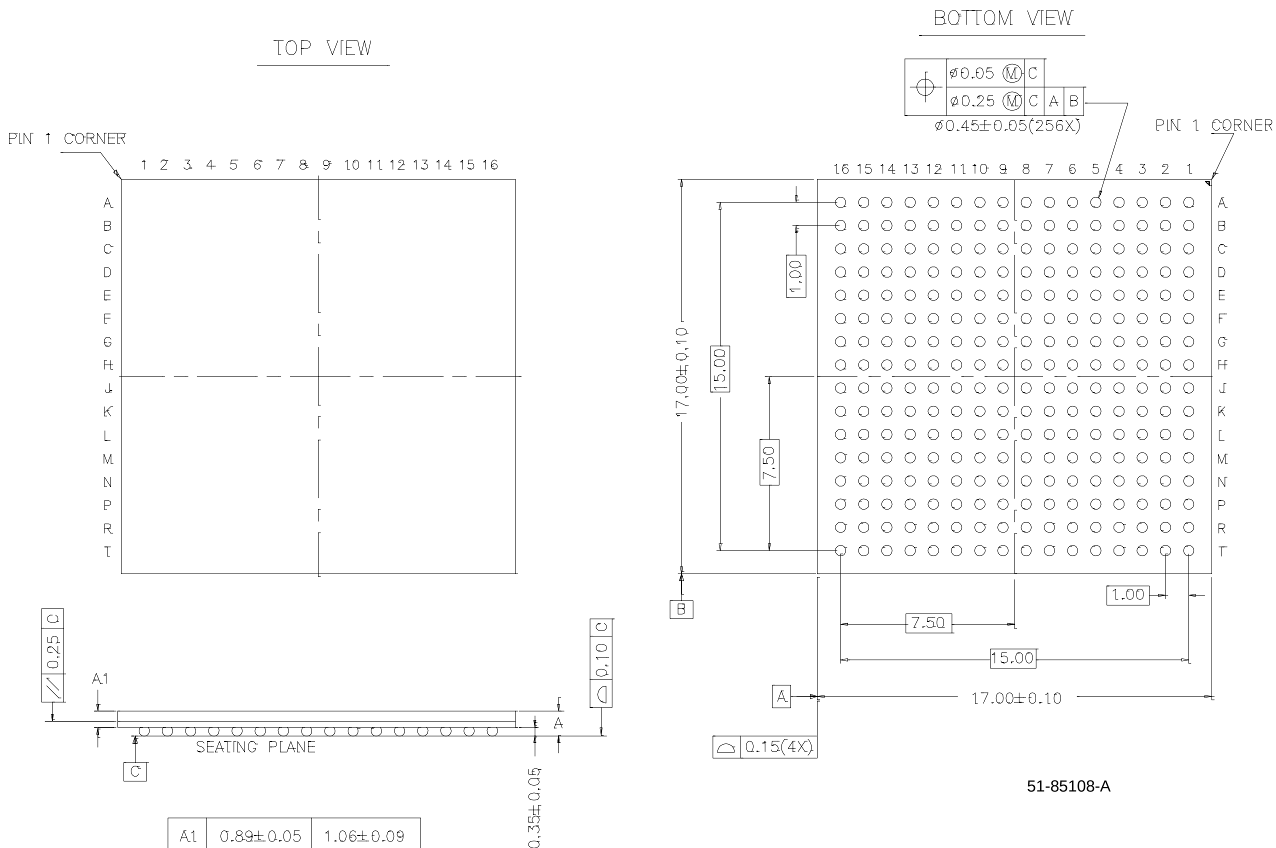
256-Lead Ball Grid Array (27 x 27 x 2.33 mm) BG256



51-85097

Package Diagrams (continued)

256-Ball Thin Ball Grid Array (17 x 17 mm) BB256

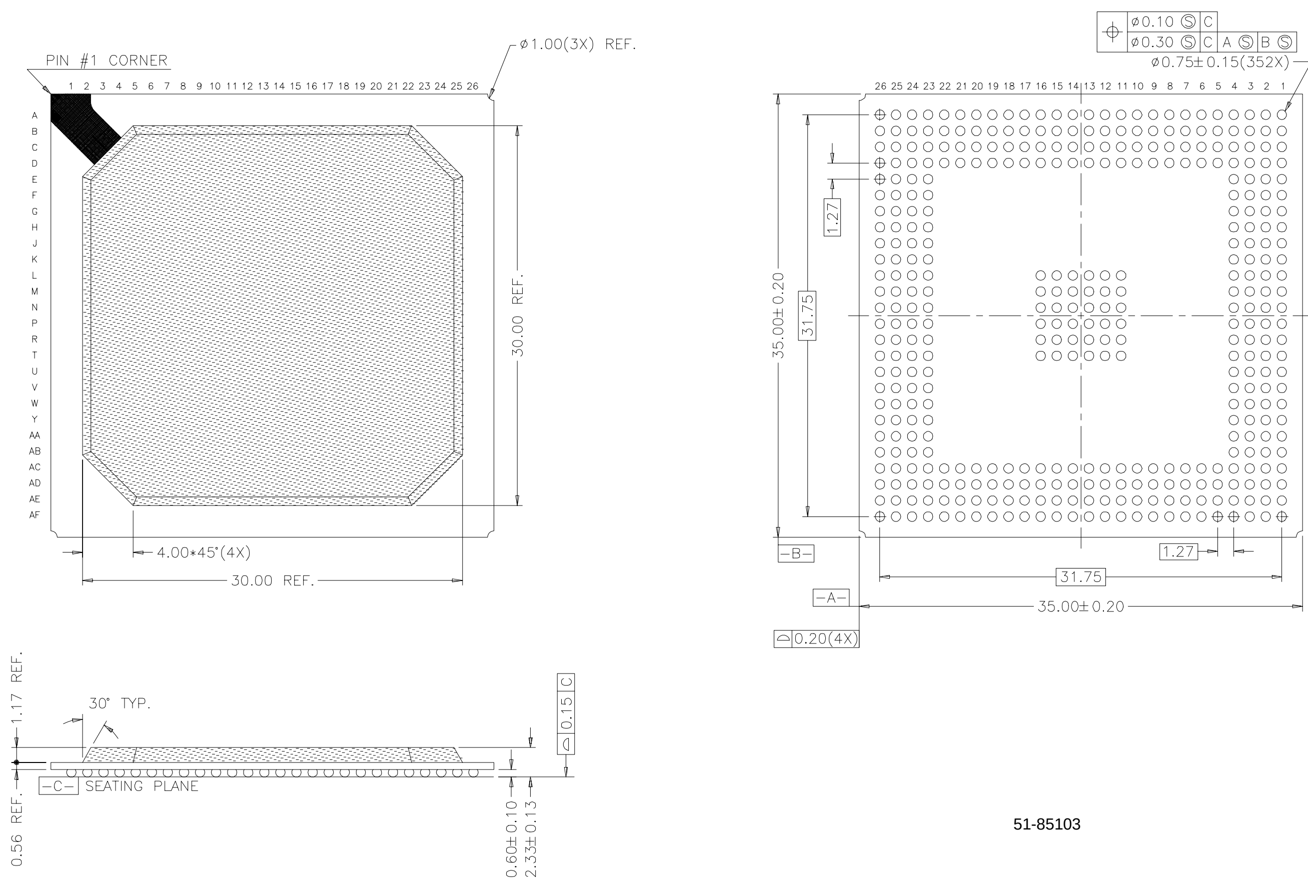


A1	0.89±0.05	1.06±0.09
A	1.40 MAX.	1.60 MAX.

51-85108-A

Package Diagrams (continued)

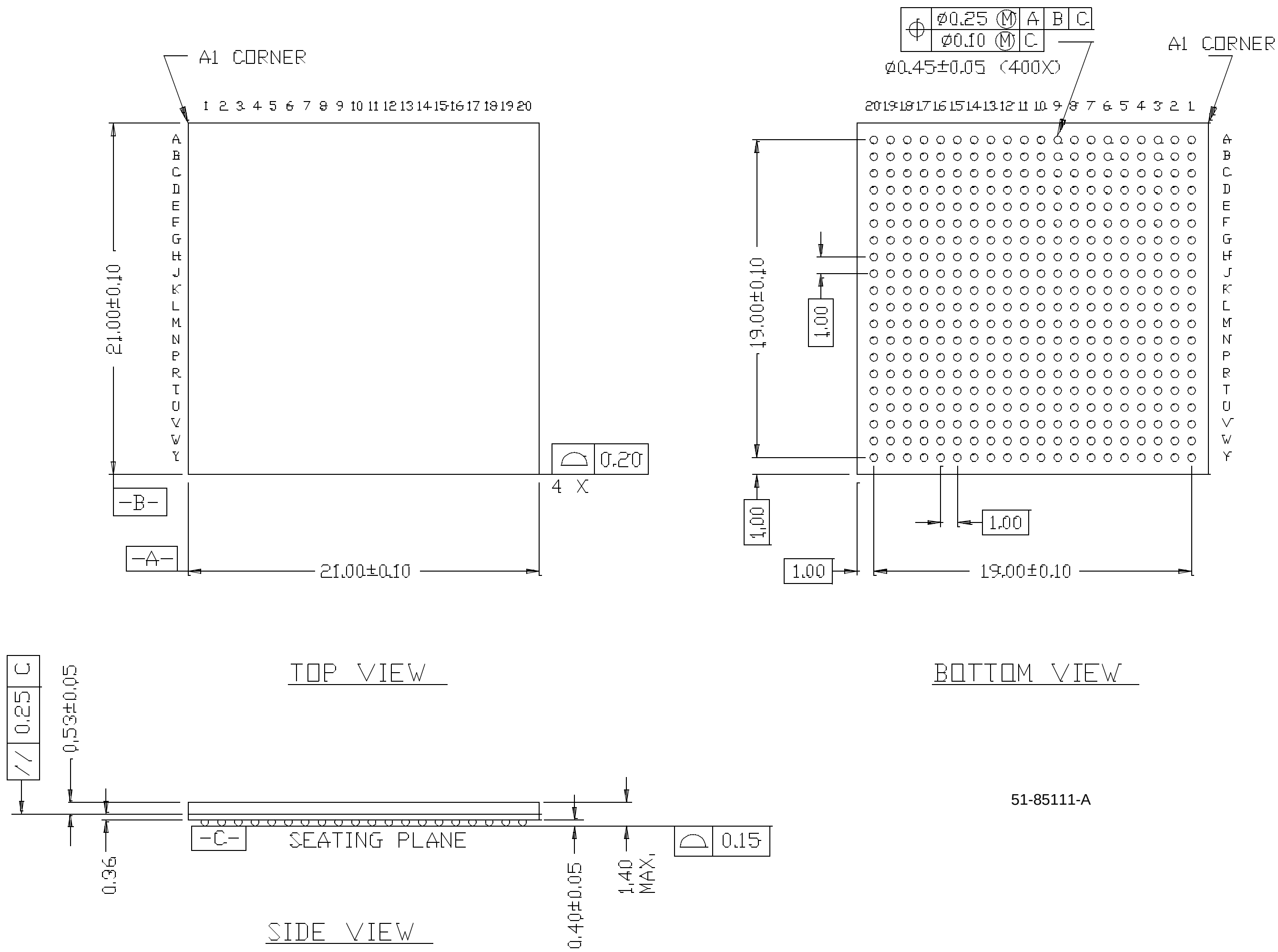
352-Lead Ball Grid Array (35 x 35 x 2.33 mm) BG352



51-85103

Package Diagrams (continued)

400-Ball FBGA (21 x 21 x 1.4 mm) BB400



51-85111-A